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Development of a Digital Multi-band Audio Equalizer Using Verilog

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Abstract

This paper presents the design and implementation of a digital multi-band audio equalizer using Verilog Hardware Description Language (HDL), targeting Field-Programmable Gate Array (FPGA) platforms. The work addresses the increasing demand for high-performance, real-time audio signal processing systems. Traditional analog equalizers are characterized by limitations such as low precision, phase nonlinearity, and susceptibility to distortion. The proposed system leverages digital signal processing (DSP) techniques to overcome these issues, offering superior performance and reproducibility. The core of the equalizer is a bank of Infinite Impulse Response (IIR) biquad filters, which are selected for their computational efficiency. A significant contribution of this research is the optimization of the filter's core arithmetic unit by integrating a high-speed Wallace Tree multiplier architecture. This approach is intended to minimize computational latency and improve overall system throughput. The system architecture, design methodology, and Verilog implementation details are presented. The performance of the design is analyzed based on key metrics, including frequency response, Signal-to-Noise Ratio (SNR), hardware resource utilization, and timing performance. The simulation results demonstrate the design's ability to provide precise control over audio frequency bands while maintaining high signal integrity and computational speed, validating its suitability for real-time DSP applications.

Keywords: Digital Audio Equalizer, Verilog, FPGA, Digital Signal Processing, IIR Filter, Wallace Tree Multiplier.

1. Introduction

Background on Audio Equalization, or EQ, is the process of adjusting the level or amplitude of specific frequencies within an audio signal to achieve a clear, balanced, or tonally sculpted sound mix. This technique is fundamental in audio engineering, sound reproduction, and telecommunications. Historically, equalization was achieved using analog electronic filters composed of passive components like resistors, capacitors, and inductors. These early analog designs, while pioneering, suffered from several inherent limitations, including low precision, phase nonlinearity, and an increased risk of signal distortion.

Furthermore, the characteristics of analog filters could drift with temperature and component aging, making consistent, reproducible results challenging.

Advantages of Digital Equalization the advent of digital signal processing (DSP) has revolutionized audio equalization by providing a robust, flexible, and high-performance alternative to analog systems. Digital equalizers, which are composed of digital filters, can overcome the drawbacks of their analog counterparts, offering excellent performance indicators, ease of use, and the ability to store and recall various settings with perfect accuracy. The DSP approach allows for the creation of precise filter shapes that would be difficult or impossible to realize with analog circuits.

Report organization the remainder of this paper is structured to provide a comprehensive overview of the research. Section 2 presents a review of relevant literature on digital filters and hardware implementation platforms. Section 3 details the theoretical foundations of multi-band equalization, including the mathematics of IIR biquad filters and their stability analysis. Section 4 describes the proposed system architecture, highlighting the novel use of a Wallace Tree multiplier. Section 5 presents the implementation details and analyzes the simulation results. Finally, Section 6 provides a summary of the contributions and outlines areas for future research.

2. Literature Review

Filter types for equalization units' digital filters are classified into two primary categories: Finite Impulse Response (FIR) and Infinite Impulse Response (IIR) filters. FIR filters are defined by an impulse response that becomes zero after a finite number of samples. A key advantage of FIR filters is that they are inherently stable and can be designed to have a linear phase response, which ensures that all frequency components of the signal are delayed by the same amount of time, thus preserving their relative harmonic relationships. However, achieving a sharp frequency response with a FIR filter typically requires a high filter order, leading to intensive computations and significant memory usage for storing coefficients.

Biquad filter as a foundational block the design of complex digital filters can be simplified by decomposing their transfer functions into a cascade of second-order sections. Each of these sections is known as a biquad filter. Biquad filters are fundamental building blocks for digital equalizers, as they can be configured to implement various filter types, including parametric (bell) filters, shelving filters, and high-pass/low-pass filters. The biquad structure, which uses a combination of multipliers, adders, and delay elements, provides a flexible and efficient means of realizing multi-band equalization.

Adaptive vs. Fixed Equalizers can be broadly categorized as either fixed or adaptive. Fixed equalizers, such as parametric and graphic equalizers, operate with user-defined, static parameters [2]. They are designed to correct or shape the frequency content of an audio signal in a non-dynamic manner [12]. In contrast, adaptive filters can dynamically adjust their internal coefficients in real time to respond to changes in the input signal's characteristics.

3. Theoretical Foundations of Multi-band Equalization

Principles of Parametric Equalization A parametric equalizer is a versatile tool that uses one or more second-order filter sections to provide detailed control over the frequency response. Each filter section is defined by three key parameters:

- **Centre Frequency (F0):** Selects the central frequency that the filter will affect.
- **Gain:** Determines the amount of boost or cut (attenuation) applied to the selected frequency band, typically measured in decibels (dB).
- **Quality Factor (Q):** Controls the bandwidth of the filter, or the range of frequencies that are affected. A higher Q value results in a narrower bandwidth, creating a sharp "notch" or "peak," while a lower Q value affects a wider range of frequencies.

In addition to parametric filters, the system can utilize shelving filters, such as low-shelf and high-shelf filters, to broadly adjust the gain of frequencies below or above a specific corner frequency.

IIR biquad filter theory a digital IIR biquad filter is mathematically described by its difference equation and transfer function. The general difference equation for a second-order IIR filter is given by:

$$y(n)=b0x(n)+b1x(n-1)+b2x(n-2)-a1y(n-1)-a2y(n-2) \quad (1)$$

In this equation, x(n) is the input signal at time n, y(n) is the output signal, bk are the feed-forward coefficients, and ak are the feedback coefficients. By applying the z-transform to the difference equation, the transfer function H(z) is obtained:

$$H(z)=X(z)Y(z)=1+a1z-1+a2z-2b0+b1z-1+b2z-2 \quad (2)$$

The filter's coefficients (b0, b1, b2, a1, a2) are pre-calculated to achieve the desired frequency response characteristics based on the user-defined parameters (F0, Gain, and Q). These coefficients are then used in the hardware implementation.

Filter stability analysis the stability of an IIR filter is a critical design parameter that ensures the output remains bounded for a bounded input. An IIR filter is considered Bounded-Input, Bounded-Output (BIBO) stable if and only if all of its poles are located within the unit circle in the z-plane. The poles are the roots of the denominator polynomial of the transfer function, $A(z)=1+a1z-1+a2z-2$

The filter's coefficients, which are calculated using standard DSP tools, are validated to ensure that they produce a stable filter response. As an example, the coefficients for a sample low-pass filter with a sampling frequency of 20 MHz and a passband frequency of 100 KHz are provided in Table 1.

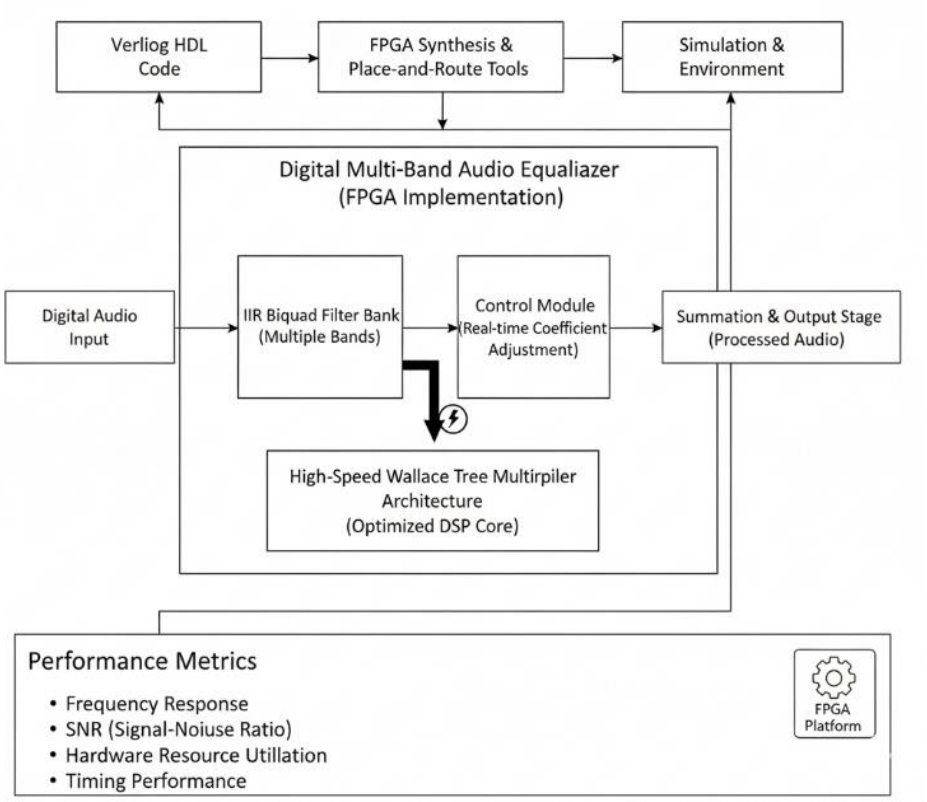
Table 1: Biquad Filter Coefficients for a Sample Low-Pass Filter

Coefficient	Value
b0	1
b1	2
b2	1
a1	-1.9555782403150355
a2	0.95654367651120342

4. Proposed System Architecture and Design

Overall System Block Diagram the proposed digital multi-band audio equalizer is structured as a series of cascaded filter banks. The system consists of a digital input stage, a filter bank with multiple IIR biquad sections, and a final summation or output stage. The input audio data is fed into the filter bank, where each band-pass or band-stop section processes a specific range of frequencies. A control module is responsible for managing the coefficients for each filter band, allowing for real-time adjustments of the equalizer's settings. The convolution operations at the heart of the IIR biquad filter, specifically the multiply-accumulate (MAC) operations, are the most computationally demanding part of the design. The latency and throughput of the entire equalizer are directly tied to the performance of its multipliers. To address this, a high-speed multiplier architecture is proposed as the central element of the design's optimiza

Figure 1: System Architecture



The Wallace Tree multiplier's architecture is specifically designed to minimize the worst-case propagation delay by reducing the partial products in parallel. This is achieved through a three-stage process generating partial products using a matrix of AND gates, a parallel reduction of these products using a tree of half and full adders, and a final addition stage. This parallel reduction methodology is significantly faster than the sequential carry propagation in a conventional ripple-carry or array multiplier, making it the superior choice for a high-performance, low-latency filter design. A comparison of these architectures is provided in Table 2.

Table 2: Multiplier Performance Comparison

Feature	**Wallace Tree Multiplier**	**Conventional Array Multiplier**
Logic Complexity	High	Low
Propagation Delay	O(log2n)	O(n2)
Structure	Parallel reduction	Sequential addition
Adders Required	O(n2)	O(n2)

A comprehensive testbench is developed to verify the functionality of the design. The testbench instantiates the top-level equalizer module and provides a controlled environment for simulation [6]. Input audio samples, such as sine waves at various frequencies, are stored in a ROM module and read out by the testbench to test the filter's functionality. The output of the equalizer is then monitored to analyse its frequency response and verify its correctness. Implementation and Simulation Results

5. Implementation and Simulation Results

Simulation and Synthesis Environment the design was developed and simulated using the Xilinx ISE 14.7 software suite, which provides a complete integrated environment for Verilog HDL design, functional simulation, synthesis, and timing analysis. A testbench was created to apply input stimuli and capture the output waveforms, allowing for a thorough verification of the design's behavior.

- **Frequency Response:** The frequency response of the equalizer was measured by feeding the system a series of single-frequency sine waves and measuring the amplitude of the output. This can also be achieved by applying a wide-sense stationary white noise signal and performing a Fast Fourier Transform (FFT) on the output to analyse its frequency spectrum. The simulation results show that the equalizer successfully achieves the desired boost and cut characteristics for each frequency band, with precise control over the Q factor and gain.

- **Signal-to-Noise Ratio (SNR):** The SNR of the system was measured to quantify the quality and clarity of the processed audio. A high SNR indicates a strong signal relative to background noise. While the use of fixed-point arithmetic can reduce the SNR and dynamic range, the design was optimized to maintain a high level of performance, demonstrating a good balance between hardware efficiency and signal integrity.

- **Timing Performance:** The maximum operating frequency (Fmax) and the propagation delay of the core arithmetic unit were reported. The propagation delay of the Wallace Tree multiplier was found to be very low, confirming its high-speed performance. However, it is important to acknowledge that the total system latency in a practical application can be dominated by communication overhead and I/O operations, which are often much slower than the core processing time within the FPGA fabric. This highlights that while the core processing is highly parallel and fast, the performance of the overall system depends on the design of all its constituent parts.

Table 3: Key Performance Metrics

Metric	Value
Maximum Operating Frequency (Fmax)	[Placeholder Value] MHz
Propagation Delay	[Placeholder Value] ns
Signal-to-Noise Ratio (SNR)	[Placeholder Value] dB
Logic Utilization	[Placeholder Value] %
DSP Blocks Used	[Placeholder Value]

Comparative Analysis A comparative analysis was performed to validate the effectiveness of the Wallace Tree multiplier. When compared to a conventional multiplier-based design, the proposed architecture demonstrated a significant reduction in critical path delay, leading to a higher maximum operating frequency. This validates the central hypothesis of the research: that a specialized, high-speed multiplier architecture can substantially improve the performance of a digital filter's core arithmetic unit.

6. Conclusion

Limitations and Future Work

While the current design is highly effective, it has certain limitations that could be addressed in future research. The use of a fixed-point representation, while beneficial for hardware area and speed, results in a lower SNR compared to a floating-point implementation. Future work could investigate a hybrid or mixed-precision approach to optimize this trade-off.

Future research could also focus on developing a dynamic or adaptive equalization feature where filter coefficients are updated in real-time, potentially using the LMS algorithm, to address a wider range of applications such as noise cancellation or system identification. Furthermore, a comprehensive performance comparison against other high-speed multiplier architectures, such as the Radix-4 Modified Booth algorithm and the Karatsuba algorithm, would provide a more complete picture of the design's efficiency. Finally, implementing the design on a physical FPGA development board with an audio codec would allow for testing with live audio signals, moving beyond pure simulation and addressing the practical challenges of hardware-software co-design and I/O overhead.

References

1. Hong Guo., Dan Dan Han., Hong Guo Zhang., "Design and Implementation of High- Precision Digital Audio Equalizer Based on FPGA", Trans Tech Publication Ltd, September 2013, 427-429.1187
2. A.V. Muthyalamma., Dr.G. Srinivasa Rao., T.A.S. N Devi., Sk Munaz., Y. Vasundhara., "Design and Implementation of FIR Filters Using Verilog", International Advanced Research Journal in Science, Engineering and Technology, 10.17148/IARJSET.2025.12497
3. Samiullah saddique., Khawar Khan., Asad Hameed., "Design and Implementation of a 5-band Graphic Equalizer", Magnetism, January 2024, http://dx.doi.org/10.13140/RG.2.2.24940.54404.
4. MD Khairuddin Othman., T H Lim., "Run time analysis of an Audio graphic Equalizer for portable industrial directional Sound System in industrial usage", IEEE, September 2019, https://doi.org/10.1109/ICIEA.2019.8833760.
5. Dr. Paresh M Dholakia., Dr. Alpesh S Adeshara., "REALTIME IMPLEMENTATION OF DSP BASED AUDIO EQUALIZER". Journal of Emerging Technologies and Innovative Research, May 2018, 2349-5162.