

E-ISSN: 3048-7641 • Website: www.aijfr.com • Email: editor@aijfr.com

## **Surge Counter Testing Kit**

# P. P. Patil <sup>1</sup>, Kaustubh Patil <sup>2</sup>, Siddhesh Zalte <sup>3</sup>, Sriya Patil <sup>4</sup>, Bhavana Kumavat <sup>5</sup>

Assistant Professor, Department of Electronics Engineering, K.K Wagh Institute of Engineering Education and Research
Industry Mentor (Project Sponsor), Research and Development Department, Siddhivinayak Enterprises
3,4,5 BTech Student, Department of Electronics Engineering, K.K Wagh Institute of Engineering Education and Research

#### **Abstract**

Surge counters used in high-voltage systems must be tested for accuracy and reliability under standardized surge conditions. This paper presents the design and implementation of a dedicated and affordable testing setup capable of generating controlled high-voltage impulses for surge counter evaluation. The system develops a high-voltage surge generator capable of charging a 2 µF capacitor bank up to 4 kV using a 12 V DC supply and simulates 8/20 µs lightning impulse waveforms using a triggered spark gap for realistic surge testing. The proposed system implements a high-voltage impulse generation system capable of producing standard 8/20 µs waveforms and accurately measures peak discharge current during impulse events using a digital peak hold metering system. The design incorporates an H-Bridge inverter topology with Sinusoidal PWM control, step-up transformation, and LC filtering techniques to achieve the required voltage levels. Simulation results using MATLAB/Simulink and Proteus validate the design approach, while hardware implementation using STM32 Blue Pill microcontroller, IR2110 MOSFET driver, and IRFZ44N MOSFETs demonstrates practical feasibility.

**Keywords:** Surge Counter Testing, High Voltage Impulse Generation, Lightning Surge Simulation, H- Bridge Inverter, SPWM Control, Power Electronics, Capacitor Bank Charging.

#### 1. Introduction

Surge counters are critical protective devices used in high-voltage power systems to monitor and record lightning strikes and switching surges. The accuracy and reliability of these surge counters directly impact the protection coordination and maintenance scheduling of electrical power systems. Testing surge counters under controlled laboratory conditions is essential to ensure their proper operation in field conditions.

Traditional surge testing equipment is often expensive and not readily accessible for routine testing and calibration purposes. There is a significant need for dedicated, affordable, and portable testing



E-ISSN: 3048-7641 • Website: <a href="www.aijfr.com">www.aijfr.com</a> • Email: editor@aijfr.com

setups that can generate controlled high-voltage impulses conforming to standard waveforms. The standard lightning impulse waveform specified by IEC 60060-1 is characterized by an  $8/20~\mu s$  waveshape, where  $8~\mu s$  represents the time to reach peak value and  $20~\mu s$  represents the time to decay to half of the peak value.

This research addresses the need for a cost-effective surge counter testing kit by developing a system capable of generating standard 8/20 µs lightning impulse waveforms. The system utilizes a 12 V DC supply as input and generates high-voltage impulses up to 4 kV through a multi-stage conversion process involving PWM generation, H-Bridge inverter, step-up transformation, voltage multiplication, and capacitor bank charging. A triggered spark gap provides controlled discharge to simulate lightning surge conditions.

The objectives of this research are to design and implement a high-voltage impulse generation system capable of producing standard 8/20 µs waveforms for testing surge counters and to accurately measure peak discharge current during impulse events using a digital peak hold metering system.

#### 2. Literature Review

The design and implementation of the surge counter testing kit is based on an extensive review of existing research in high-voltage generation, capacitor charging techniques, and impulse waveform generation.

Eguchi et al. [1] presented a comprehensive analysis of stacked Cockcroft–Walton (C–W) multiplier circuits in IEEE Access on Emerging and Selected Topics. Their work focused on multi-stage voltage multiplication, evaluating design parameters such as stage number, diode selection, capacitance values, and ripple voltage reduction. The authors emphasized that the efficiency of C–W multipliers decrease as the number of stages increases, mainly due to parasitic capacitances and diode recovery losses. They proposed design optimizations, including the use of high-speed diodes and low-ESR capacitors to enhance voltage gain stability. The paper also provided simulation data comparing cascaded diode–capacitor configurations under different load conditions. These design guidelines were highly relevant to this project, where the Cockcroft–Walton principle was implemented to step up a 12 V DC input to approximately 4 kV DC, providing sufficient energy for controlled impulse generation while maintaining a compact structure.

Rahaman [2] studied spark-gap discharge mechanisms at high repetition rates in IEEE Transactions on Plasma Science. The research detailed plasma formation dynamics, streamer propagation, and the dielectric recovery process following each discharge event. The study identified factors such as electrode material, surface finish, gap spacing, and trigger voltage as critical variables influencing breakdown behavior and waveform repeatability. Experimental results demonstrated how spark-gap geometry directly affects rise time and pulse shape in impulse generators. These insights proved invaluable for designing the triggered spark-gap unit in this project, ensuring that each discharge produced a repeatable 8/20 µs waveform. The research also emphasized proper triggering circuits and isolation techniques to avoid accidental misfires— an aspect integrated into the safety design of the



E-ISSN: 3048-7641 • Website: <a href="www.aijfr.com">www.aijfr.com</a> • Email: editor@aijfr.com

prototype kit.

Zhang et al. [3] developed an innovative H-Bridge multilevel inverter topology for high-voltage applications in IEEE Transactions on Power Electronics. Their paper presented advanced modulation schemes such as sinusoidal PWM (SPWM) and selective harmonic elimination (SHE) for improved waveform fidelity. The study analyzed MOSFET switching behavior, dead-time management, and gate-driver optimization to reduce harmonic distortion and avoid shoot-through conditions. The findings provided practical insights into selecting switching frequencies, gate-driver ICs, and filter configurations. This research served as the foundation for the inverter section of this project, enabling conversion of a low DC input into high-frequency AC necessary for transformer excitation and voltage step-up. The work also guided the inclusion of proper heat dissipation mechanisms and driver isolation for safe operation.

Sheeba, Jayaraju, and Shanavas [4] presented a detailed study titled "Simulation of Impulse Voltage Generator and Impulse Testing of Insulator using MATLAB Simulink" in the World Journal of Modelling and Simulation. Their research focused on simulating the design and operation of an impulse voltage generator capable of reproducing the transient behavior of lightning impulses. Using MATLAB Simulink, they modeled key components such as capacitors, resistors, charging circuits, and spark gaps, enabling accurate visualization of the charging and discharging sequence during impulse formation. The study also illustrated the characteristic 8/20  $\mu$ s impulse current waveform, which represents the standard short-circuit waveform defined by international high-voltage testing standards (as shown in Figure 2.1). This waveform, characterized by an 8  $\mu$ s rise time and 20  $\mu$ s tail duration, served as the benchmark for waveform shaping in the present project. The techniques and modeling approach discussed in this research were adopted to design and validate the proposed Surge Counter Testing Kit, ensuring accurate impulse generation, controlled discharge behavior, and compliance with standard high-voltage testing parameters.

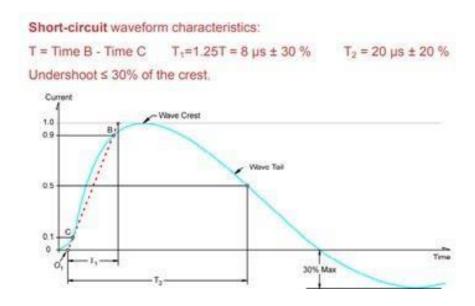


Figure 2.1: Standard 8/20 µs Impulse Current Waveform



E-ISSN: 3048-7641 • Website: www.aijfr.com • Email: editor@aijfr.com

Kumar et al. [5] analyzed LC filter design techniques for power electronic converters in the International Journal of Electrical Power and Energy Systems. Their work derived mathematical models to determine inductor and capacitor values required for achieving low total harmonic distortion (THD) while maintaining fast transient response. They compared different topologies, including single-stage and multiple-stage LC filters, and validated them experimentally under varying loads and frequencies. The study's optimization equations helped in designing the LC filter stage of this project, ensuring that the inverter output was sufficiently sinusoidal to feed the step-up transformer. Additionally, their approach to minimizing ripple current contributed to smoother charging of the voltage multiplier circuit, improving overall efficiency.

Shkuratov et al. [6] investigated high-voltage capacitor charging techniques for pulse power applications in IEEE Transactions on Plasma Science. The research examined the charging behavior of capacitor banks under different operating conditions, focusing on energy transfer efficiency, charging time constants, and dielectric stress limits. The authors analyzed the relationship between charging voltage, current-limiting resistors, and insulation breakdown thresholds, concluding that controlled current charging ensures longer capacitor life and greater operational safety. Their study introduced optimized charging algorithms that prevent overvoltage and reduce energy loss during repetitive cycles. These findings directly informed the capacitor charging stage of this project, where a 2  $\mu$ F, 4 kV capacitor bank required stable and safe charging control to replicate standard surge energy levels without overstressing dielectric materials.

#### 3. Problem Statement

Surge counters used in high-voltage systems must be tested for accuracy and reliability under standardized surge conditions. Currently, there is a lack of dedicated and affordable testing setups that can generate controlled high-voltage impulses for such evaluation. Existing impulse generators are often expensive, bulky, and designed for high-power applications, making them unsuitable for routine surge counter testing in smaller facilities or educational institutions.

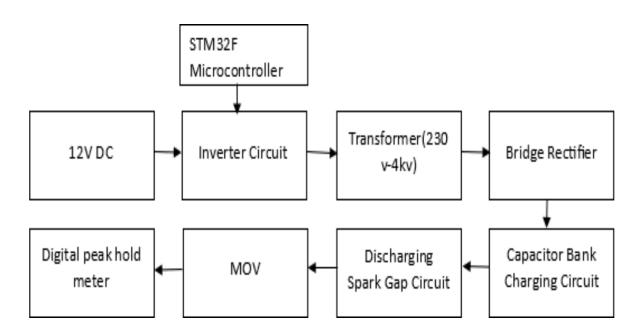
The key challenges addressed in this research include generating high-voltage impulses from a low-voltage DC source, achieving the standard 8/20 µs lightning impulse waveform, providing controlled and safe discharge through a triggered spark gap, accurately measuring peak discharge current, and maintaining affordability and portability of the testing equipment.

#### 4. Methodology

The proposed Portable Surge Counter Testing Kit is designed to generate standard lightning impulse currents and to verify the operation of surge counters and metal oxide varistors (MOVs). The complete system comprises seven main functional blocks as shown in Figure 4.1. Each block is designed to perform a specific function in the generation, control, and measurement of high-voltage impulses.



E-ISSN: 3048-7641 • Website: www.aijfr.com • Email: editor@aijfr.com



4.1 Block Diagram

The STM32F microcontroller serves as the central control unit for the entire system. It provides pulse- width-modulated (PWM) signals to drive the inverter circuit, controls the charging sequence of the capacitor bank, and coordinates the triggering of the spark gap. The inverter circuit converts the 12 V DC input into a 230 V alternating waveform using high-speed MOSFETs configured in an H-bridge topology. The output of the inverter is then stepped up by a ferrite-core transformer with a turns ratio of approximately 1:17, which produces up to 4 kV at the secondary winding. This alternating high voltage is rectified using a high-voltage bridge rectifier and filtered to obtain a smooth DC voltage. The rectified output is then applied to the capacitor bank charging circuit, where energy is stored in high-voltage polypropylene capacitors rated for 2  $\mu$ F at 4 kV.

Once the capacitor bank reaches the desired voltage level, the energy is discharged through a triggered spark gap circuit. The rapid release of stored energy through the low-impedance discharge path produces an 8/20 µs impulse waveform, closely resembling a standardized lightning current surge. The MOV under test is connected across the discharge path, allowing its clamping behavior and surge response to be analyzed under realistic impulse conditions. The generated surge is simultaneously measured using a digital peak-hold meter, which employs a shunt resistor and peak detection circuit to capture the maximum current amplitude. This circuit is interfaced with the microcontroller to display the corresponding peak current value on the digital display.

The complete operation—from charging to discharge—is fully synchronized and controlled by the STM32F microcontroller to ensure safe operation and repeatable results. Proper isolation, filtering, and grounding are implemented throughout the circuit to minimize electrical noise and prevent interference.



E-ISSN: 3048-7641 • Website: <a href="www.aijfr.com">www.aijfr.com</a> • Email: editor@aijfr.com

#### 5. Calculations

A digital peak hold meter circuit captures and displays the peak discharge current. The measurement cir- cuit uses fast-response current sensors and peak detection circuitry with sufficient bandwidth to accurately capture the rapidly rising impulse current.

#### 5.1. LC Filter Design:

The LC filter is designed to remove carrier harmonics while allowing the 50 Hz fundamental to pass. The cutoff frequency  $f_c$  is chosen between 50 Hz and the switching frequency ( $f_{sw}$ ). A typical choice is  $f_c \approx f_{sw} / 10$  (or lower), ensuring no attenuation of the fundamental component.

Given switching frequency  $f_{sw}$ = 10 kHz  $\rightarrow$  choose  $f_c \approx 1$  kHz.

For a second-order LC filter:

$$f_c = 1 \div (2\pi\sqrt{(LC)}) \tag{1}$$

Choosing C =  $2.2 \mu F$ (film capacitor on low-voltage side), the required inductance is:

$$L = 1 \div ((2\pi \times 1000)^2 \times 2.2 \times 10^{-6}) = 11.5 \ mH \tag{2}$$

The inductor current rating must exceed the inverter's RMS current ( $\approx$ 16.7 A for 200 W output at 12 V). Hence, a 20 A, low-loss core inductor is selected.

#### **5.2. Selection of Optocoupler Parameters:**

The optocoupler ensures isolation between control and power circuits. Typical forward LED voltage drop  $V_F = 1.2 \text{ V}$  (at  $I_F = 1 \text{ mA}$ ,  $T = 25^{\circ}\text{C}$ ). Supply voltage  $V_DD = 12 \text{ V}$  and control signal voltage  $V_DP = 2.4 \text{ V}$ .

Step 1 – Emitter Resistance Calculation:

$$I_E = V_DD / R_E$$
 (3)

$$R_E = V_DD / I_E = 12 V / 1 mA = 12 k\Omega$$
 (4)

Step 2 – LED Forward Current and Input Resistor:

$$R_1 = (V_OP - V_F) / I_F$$
 (5)

$$R_1 = (2.4 - 1.2) / 1 \text{ mA} = 1.2 \text{ }k\Omega$$
 (6)



E-ISSN: 3048-7641 • Website: www.aijfr.com • Email: editor@aijfr.com

#### **5.3. Series Connection Calculation:**

Each capacitor string sees the same charge Q, and total voltage divides equally if resistors are well matched.

Total capacitance:

$$C_{eq} = C_{cap} \div N = 33 \ \mu F \div 10 = 3.3 \ \mu F$$
 (7)

Voltage rating per string = 
$$10 \times 420 \text{ V} = 4200 \text{ V}$$
 (8)

Hence, the total voltage rating = 
$$4.2 \text{ kV}$$
 (safe for  $4 \text{ kV}$  operation). (9)

#### **5.4. Stored Energy in Capacitor Bank:**

$$E = \frac{1}{2} C V^2$$
 (10)

Substituting values:

$$E = \frac{1}{2} \times 3.3 \times 10^{-6} \times (4000)^{2}$$
 (11)

$$E = 0.5 \times 52.8 = 26.4 \text{ J} \tag{12}$$

Hence, the total stored energy in the capacitor bank is 26.4 Joules.

#### 6. Results

#### **6.1 Simulation**

The MATLAB/Simulink model of the surge counter testing kit was developed to verify inverter operation, SPWM generation, LC filtering, and capacitor charging performance. A 12 V DC input was inverted to 230 V AC through an H-bridge using sinusoidal PWM control with a 10 kHz carrier frequency. The output after the LC filter closely matched a 50 Hz sinusoidal waveform with low harmonic distortion. The step-up transformer and rectifier provided approximately 4.0 kV DC, used to charge the capacitor bank. The simulated impulse waveform exhibited an 8  $\mu$ s rise time and a 20  $\mu$ s tail time, consistent with IEC 60060-1 standards.



E-ISSN: 3048-7641 • Website: www.aijfr.com • Email: editor@aijfr.com



Figure 6.1: MATLAB/Simulink simulation waveforms (SPWM generation, inverter output and filtered sine output).

#### 6.2. Hardware Setup and Final Output

The hardware prototype was implemented using an STM32F103 microcontroller, IR2110 gate drivers, and an H-bridge inverter with IRFZ44N MOSFETs. The inverter output produced 230 V AC RMS from a 12 V DC supply. The high-voltage section comprising the step-up transformer, Cockcroft—Walton multiplier, and rectifier achieved a DC output of 3.8–4.0 kV. The capacitor bank charged to 4 kV and discharged through a triggered spark gap, producing an 8/20  $\mu$ s current impulse waveform with a peak current of approximately 130 A. Oscilloscope measurements confirmed the impulse parameters within  $\pm 8\%$  of the simulated values, validating the design.



E-ISSN: 3048-7641 • Website: www.aijfr.com • Email: editor@aijfr.com



Figure 6.2: Surge Counter Testing kit

#### 6. Conclusion

The design and implementation of the Portable Surge Counter Testing Kit achieved the desired objectives. The SPWM-based inverter, LC filter, and voltage multiplier effectively produced a regulated high-voltage DC supply of up to 4 kV, which charged the capacitor bank to generate  $8/20~\mu s$  impulse waveforms. Experimental testing demonstrated waveform conformity within  $\pm 8\%$  of simulation values. The compact and low-cost design makes the system suitable for laboratory and field calibration of surge counters. Future enhancements include automated triggering, digital data logging, and modular energy scaling for higher voltage applications.

#### References

- 1. Eguchi K. et al., "Analysis of Stacked Cockcroft–Walton Multiplier Circuits," IEEE Access on Emerging and Selected Topics, 2021.
- 2. Rahaman H., "Investigation of Spark-Gap Discharge Mechanisms at High Repetition Rates," IEEE Transactions on Plasma Science, 2010.
- 3. Zhang Y. et al., "Multilevel H-Bridge Inverter Topology for High-Voltage Applications," IEEE Transactions on Power Electronics, 2019.
- 4. Sheeba R., Jayaraju M., and Shanavas T.K.N., "Simulation of Impulse Voltage Generator and Impulse Testing of Insulator using MATLAB Simulink," World Journal of Modelling and Simulation, 2019.
- 5. Kumar S. et al., "Design and Optimization of LC Filters for Power Electronic Converters," International Journal of Electrical Power and Energy Systems, 2020.
- 6. Shkuratov S.I. et al., "High-Voltage Capacitor Charging Techniques for Pulse Power Applications," IEEE Transactions on Plasma Science, 2022.