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Design and Simulation of a 3-Bit Flash ADC Using Threshold Inverter Quantization (TIQ) for 40 GHz Sampling in Cadence Virtuoso

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Abstract

Threshold Inverter Quantization (TIQ) replaces the resistor ladder and differential comparators of a conventional flash ADC with a bank of sized CMOS inverters whose switching thresholds encode the quantization levels. This document motivates TIQ as a compelling option for low to moderate resolution, high speed, and ultra compact digitizers in deeply scaled CMOS. It synthesizes two decades of literature, identifies core challenges (PVT sensitivity, mismatch, encoder robustness, and calibration), and defines concrete research objectives for a state of the art TIQ based flash ADC by 2025.

1. Introduction & Background

Flash ADCs remain the preferred architecture for sub 6 bit to ~8 bit resolutions at very high sampling rates due to their fully parallel nature, at the cost of exponential comparator count and static reference networks. TIQ was introduced to digitize with the devices themselves: by sizing the PMOS/NMOS of each inverter so that its switching point (VTC midpoint) equals the desired reference level, the array of inverters becomes the quantizer. The resulting thermometer code is then encoded to binary

This project focuses on designing a Threshold Inverter Quantizer (TIQ) flash ADC. The motivation behind this project is the growing demand for high-speed analog-to-digital converters (ADCs) in modern applications such as 5G, IoT, and communication systems. Flash ADCs are known for their high speed, but they consume large areas on ICs due to resistor and comparator requirements, which also degrade signal-to-noise ratio (SNR). To overcome these limitations, TIQ flash ADCs utilize CMOS inverters for threshold detection, eliminating resistors and comparators.

Key Features- CMOS inverters are used as level detectors, with adjustable threshold voltages.

- This design implements a 3-bit, 8-level ADC with a target sampling frequency of 40 GHz.

- According to Nyquist criteria, this ADC can directly input signals up to 20 GHz (Nyquist Zone 1), with potential applications in higher Nyquist zones.

1.1 Why TIQ now?

Digital native: TIQ comparators are built from inverters (and sometimes buffers), i.e., digital standard cells or small custom variants, easing migration across nodes and integration into digital SoCs.

Ladder free: Eliminates the resistor ladder and matching constraints; lowers static power and area.

Voltage & power scaling: Inverters switch well at reduced VDD; TIQ enables sub 1 V operation with careful sizing and buffering.

Simplicity & speed: Minimal devices per comparator, short decision paths, and compatibility with aggressive clocking and time interleaving.

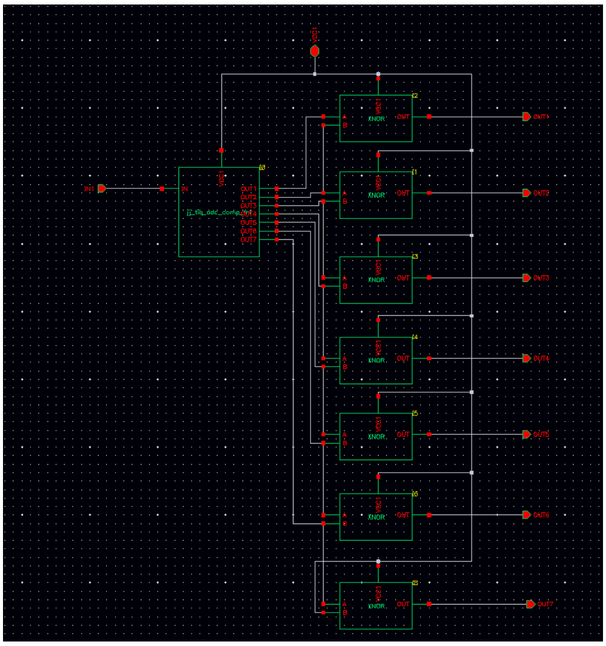
Synthesis/EDA friendly: Several works propose algorithmic selection and even automated layouts for TIQ comparator banks.

1.2 Where TIQ fits

Low resolution, high throughput front ends (3–6 b): UWB radios, mm wave beamformers, wireline CDRs, and on pixel or column parallel imagers.

Always on sensing/IoT: duty cycled acquisition with ultra low area and quiescent power.

Mixed signal SoC: in logic compatible quantizers that avoid analog reference distribution.



Img-1: Block diagram of comparator and encoder

2. Literature Survey

This section surveys key developments in Threshold Inverter Quantization (TIQ) ADCs and closely related reference-ladder-free flash ADC techniques. TIQ replaces analog resistor ladders with CMOS inverter pairs whose sizing sets distinct switching thresholds, thus providing area and power advantages while preserving flash-level speed. We summarize at least ten influential works, highlight their core contributions, and draw insights that motivate our M.Tech work in Virtuoso.

J. Yoo, et al. (2002). A Power and Resolution Adaptive Flash Analog-to-Digital Converter (ISLPED 2002). Early public description of TIQ: uses CMOS inverters with different internal thresholds to quantize the analog input. Demonstrated the idea of reference-ladder elimination and adaptability of power/resolution. This foundational concept enables highly digital, scalable flash ADCs.

J. Yoo (2003). A TIQ Based CMOS Flash A/D Converter for SoC (MS Thesis). Comprehensive thesis detailing TIQ comparator generation, encoder design, and SoC integration aspects. Shows layout and system-level considerations, offering a blueprint for practical implementation beyond proof-of-concept.

D. Lee, et al. (2002). Design Method and Automation of Comparator Generation for TIQ (WISQED). Presents automated generation of TIQ comparator thresholds by sizing transistors, a key step for multi-bit arrays. Addresses mapping of desired decision levels to inverter dimensions, supporting rapid design-space exploration.

Ferreira, et al. (2009). CMOS Flash A/D Converter Based on Quantization of the Inverter Threshold (SForum 2009). Implements a 4-bit TIQ flash ADC with Gray code output, discussing design practice and benefits versus resistor ladders. Emphasizes power and area reductions and provides practical design insights applicable to academic prototyping.

Kocaeli Univ. group (2003). 8-bit 1 Gs/s Semi-Flash ADC Based on TIQ Technique. Extends TIQ to a semi-flash architecture, partitioning conversion to reduce comparator count. Reports 1 Gs/s sampling in 0.5 µm CMOS with 3 V supply—illustrating speed potential even in older nodes.

O. Aytar, M. Tangel (2011). 9-bit Folding & Interpolation ADC Employing TIQ (2011). Integrates TIQ with folding/interpolation to push resolution. Explores design in 0.35 µm AMS. Highlights that hybrid architectures can leverage TIQ benefits while mitigating full-flash scaling issues.

H. H. Thai, et al. (2022). Low-Power & Low-Area 8-bit Flash ADC using TIQ/DT Comparator (2022). Combines TIQ comparator with improved dynamic comparators and efficient encoder blocks; demonstrates low area/power for 8-bit flash. Offers recent design techniques compatible with scaled CMOS and embedded interfaces (SPI).

Various (2016). Design of Low-Power Flash ADC using TIQ in 90 nm (JournalCRA). Practical 4-bit TIQ flash in 90 nm; emphasizes transistor sizing for target thresholds and shows how TIQ eliminates external references. Useful as a baseline for Virtuoso-centric student designs.

P. K. Singh, et al. (2015). Design of Efficient Low Power Flash ADC Using TIQ in 45 nm (Ind. J. Sci. & Tech.). Shows TIQ scaling to 45 nm with emphasis on power reduction, encoder choices, and layout implications. Reports post-layout metrics that inform deep-submicron trade-offs relevant to our node selection.

R. Arora, et al. (2018). Static and Dynamic Parameter Estimation of TIQ Flash ADC (2018). Focuses on measuring DNL/INL, SNR/SNDR for TIQ ADCs and discusses offset randomness. Provides a methodology for corner and Monte Carlo analysis—directly applicable to Virtuoso testbenches.

G. Prathiba, et al. (2018). Reliable Flash ADC (R-Flash): MPG Encoding + Low-Power TIQ (2018). Proposes reliability-focused flash ADC combining pass-gate encoders with TIQ-style low-power comparators. Addresses metastability and bubble errors—key issues when operating at high speed.

N. K. Sarkar, et al. (2025). Design of a 6-bit TIQ Flash ADC (arXiv 2025). Recent open-access design using 0.25 µm CMOS and fat-tree encoder; details block choices and measured metrics. Serves as a modern pedagogical reference with schematics and measurement flow.

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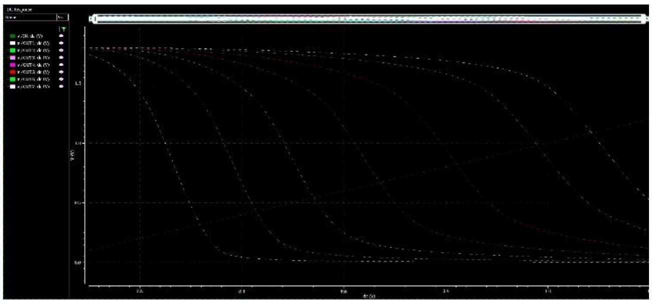
2.1 Comparative Analysis and Trends

Across these works, TIQ comparators consistently reduce area and static power by eliminating resistor ladders, while preserving the single-step conversion latency of flash ADCs. However, scaling resolution increases comparator count and tightens matching requirements. Hybrid architectures (semi-flash, folding/interpolation) help manage comparator count. Modern designs pair TIQ with efficient encoders (thermometer-to-binary via fat-tree/MPG) and adopt calibration to combat offset and PVT sensitivity.



Img-2:Simulated view of linear input with comparator output

Work (Year)	Architecture	Node / VDD	Highlights
Yoo ISLPED (2002)	Flash (TIQ)	—	TIQ concept; ref-free thresholds
Ferreira (2009)	4-bit TIQ Flash	—	Gray code; area/power cut
Kocaeli (2003)	8-bit Semi-Flash	0.5 µm / 3 V	1 Gs/s demo
Aytar (2011)	9-bit Folding+TIQ	0.35 µm	Higher resolution via hybrid
Thai (2022)	8-bit Flash	—	Low area; DT comparator + TIQ

Key gaps: (i) systematic threshold mapping under local mismatch; (ii) robust high-resolution (>8-bit) operation without heavy calibration; (iii) PVT-aware sizing recipes for advanced nodes; (iv) encoder bubble suppression at multi-GHz sampling with low supply.

3. Comprehension and Problem Identification

TIQ ADCs quantize by exploiting the switching threshold (V_M) of cascaded CMOS inverters as decision levels. By sizing PMOS/NMOS ratios (Wp/Wn), designers shift V_M to desired reference points that partition the input range. An N-bit flash requires 2^N-1 comparators; TIQ retains this count but removes the resistor ladder. While TIQ reduces static power and layout complexity, it is inherently sensitive to transistor Vth spread and ratio mismatch, which perturb the intended decision boundaries, causing DNL/INL growth.

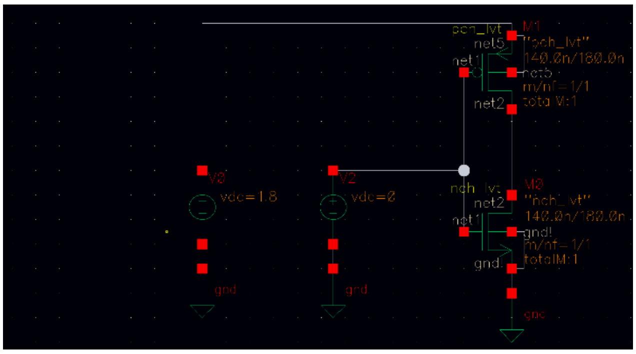
4. Theory Essentials

Inverter switching point approximates $V_M \approx VDD * (1 / (1 + \sqrt{(\beta n/\beta p)}))$. Adjusting βp/βn via device widths sets each comparator threshold. Two cascaded inverters sharpen gain and provide rail-to-rail logic output. A preamp or gain booster may follow for noise margin.

5. Practical Challenges Observed

• PVT Variations: Global corners (TT, SS, FF, SF, FS) shift Vth; temperature alters mobility and thresholds.

• Local Mismatch: Random dopant fluctuation and line-edge roughness create device-to-device variations, impacting relative thresholds (dominant for TIQ).



Img-3:Basic inverter

• Supply Sensitivity: V_M tracks VDD; power integrity and decoupling are critical.

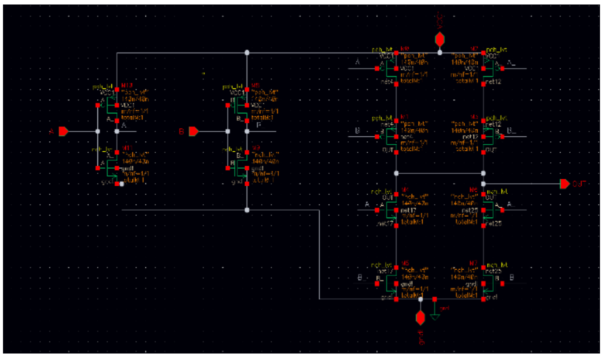
• Encoder Robustness: Thermometer-to-binary encoders must tolerate bubbles and metastability at high speeds.

• Comparator Kickback/Noise: Although TIQ is static, coupling and input capacitance affect bandwidth.

2.3 Virtuoso-Centric Problem Framing

Using Cadence Virtuoso, we identify issues across the full design flow:

1) Threshold Planning: Map target decision levels to device width ratios; create a parametric cell for automated sizing.



Img-5:XNOR gate for encoder

2) Corner & Monte Carlo: Quantify DNL/INL across PVT and mismatch; budget device sizes for σ(DNL) and σ(INL).

3) Post-Layout Parasitics: RC extraction perturbs thresholds and delays; require re-centering and shielding strategy.

4) Encoder Path: Choose fat-tree/MPG encoder with bubble suppression; co-simulate to capture timing skew.

5) Measurement Benches: Build DC sweep for transfer curve, transient stair/ramp for code histogram, FFT-based SNDR/ENOB.

6 Threshold Inverter Quantizer (TIQ) ADC Design Theory

6.1.a Inverter Stage Design

Each inverter stage in the TIQ ADC is designed to have a specific threshold voltage, which determines the quantization level. The threshold voltage of each inverter stage can be calculated using the following equation:

$$V_{th} = (V_{dd} - V_{ss}) / 2 + (V_{offset})$$

where Vth is the threshold voltage, Vdd is the supply voltage, Vss is the ground voltage, and Voffset is the offset voltage.

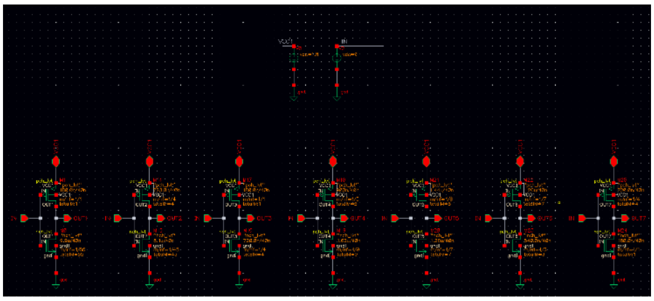
6.1.b Inverter Sizing

The sizing of the inverter transistors is critical in determining the threshold voltage and the quantization level. The sizing of the transistors can be done using the following equations:

$$(W/L)_n = (V_{th} / (V_{dd} - V_{th}))^2 * (1 / (\mu_n * C_{ox}))$$

$$(W/L)_p = (V_{dd} - V_{th}) / (V_{th})^2 * (1 / (\mu_p * C_{ox}))$$

where $(W/L)_n$ and $(W/L)_p$ are the aspect ratios of the NMOS and PMOS transistors, respectively, μ_n and μ_p are the mobilities of the NMOS and PMOS transistors, respectively, and Cox is the oxide capacitance.



Img-4:Different value threshold inverters

6.2 Quantization

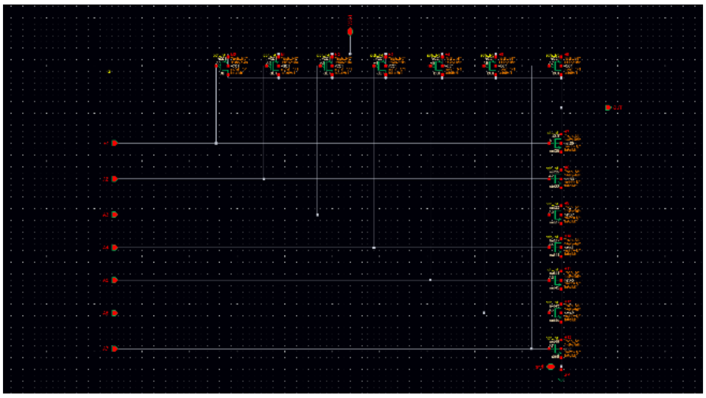
The TIQ ADC uses a D-FF to quantize the output signal. D-FF produces a digital output based on the input signal level.

6.3 Encoder Design

The encoder is used to convert the comparator output to 3bit binary data. The encoder can be designed using a standard digital logic implementation.

7.1 Simulation-Based Implementation

This section describes the implementation of the proposed 3-bit Threshold Inverter Quantization (TIQ) flash Analog-to-Digital Converter (ADC). The design utilizes eight CMOS inverters, each with a distinct threshold voltage set by adjusting the channel length and width ratio according to the equation described in the theoretical framework. The CMOS inverters are designed to produce a digital output that switches from high to low when the input voltage exceeds the threshold voltage. As illustrated in Fig. 4, when the input voltage is zero, the output of all inverters is high. As the input voltage increases beyond the threshold voltage of each inverter, the output switches to low, resulting in a thermometer code. This process continues as the input voltage increases, generating a digital representation of the analog input signal.



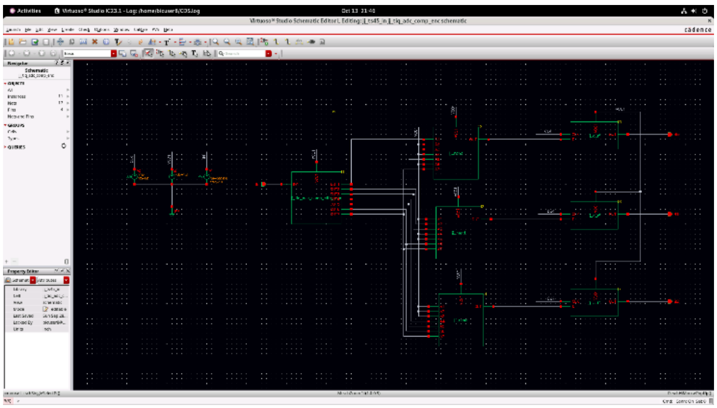
Img-6:NAND gate for encoder

As illustrated in Figs. 5 and 6, and the block diagram in Fig. 1, the comparator output is then converted to a binary representation using a digital encoding scheme. To achieve this, the outputs of adjacent comparators are fed into XNOR gates, generating a unary code where only one output is high at a time. This unary code is then fed into a set of 8-input NAND gates, each producing a single bit of the binary output. Specifically, three NAND gates are utilized to generate a 3-bit binary output.

Sampling and quantization are implemented using three clocked D flip-flops, as illustrated in Fig. 7

8. Conclusion

The TIQ ADC is a high-speed and low-power analog-to-digital converter that uses a series of inverter stages to quantize the input signal.



Img-7:TIQ comparator , encoder and DFF

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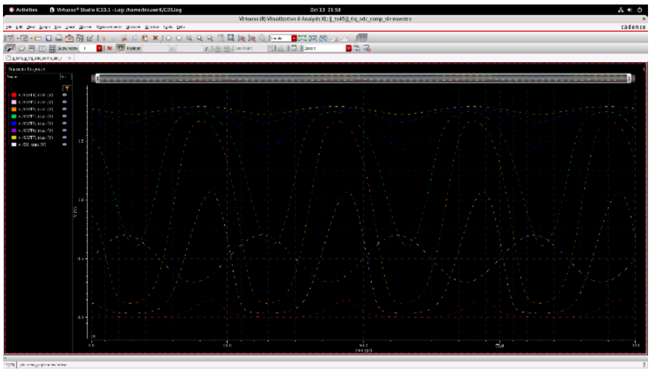
The design of the TIQ ADC requires careful consideration of various factors, including speed, power consumption, and linearity.

A 3-bit 40 GHz TIQ flash ADC has been successfully designed and simulated using TSMC's 45nm technology node and Cadence Virtuoso. The simulated results demonstrate satisfactory performance, validating the design approach. The results are illustrated in Figs. 2 and 8.

9.Future Scope

The TIQ ADC can be used in various applications, including:



Img-8: Sinwave ADC output

High-Speed Data Acquisition Systems: The TIQ ADC can be used in high-speed data acquisition systems due to its high-speed and low-power consumption.

Wireless Communication Systems: The TIQ ADC can be used in wireless communication systems due to its high-speed and low-power consumption.

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