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IoT-Enabled Remote Operated Single-to-Three Phase Variable Frequency Drive (VFD) for Precision Agriculture

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Abstract

This paper presents a **design and simulation-based validation** of an Internet of Things (IoT)-enabled, remotely operated Variable Frequency Drive (VFD) engineered to convert single-phase alternating current (AC) input into a three-phase AC output for precision agriculture applications. The system employs a full-bridge rectifier, a DC link capacitor, and an Insulated Gate Bipolar Transistor (IGBT)-based inverter topology. An ESP32 microcontroller facilitates pulse-width modulation (PWM) generation and remote-control capabilities via Wi-Fi, enabling precise speed regulation of a 1HP, 230V, three-phase induction motor. The simulation utilizes the IR2112 behavioural model and 15A/600V IGBT parameters in Proteus and MATLAB environments. Dead-time verification of 2-3 microseconds was conducted in Proteus to prevent shoot-through faults. The proposed VFD system addresses the practical constraints of rural electrification by allowing three-phase pump operation from single-phase sources, thereby enhancing water conservation through optimized pumping efficiency. This document outlines the system architecture, mathematical modelling, design calculations, and comprehensive simulation results, validating the feasibility of the ESP32-based V/f control strategy for single-to-three phase conversion before physical prototyping.

1. Introduction

Modern agriculture faces increasing pressure to optimize resource utilization, especially water, against a backdrop of fluctuating climate patterns and escalating food demands. Irrigation, a cornerstone of agricultural productivity, accounts for a substantial portion of global freshwater consumption [1][2]. Efficient water management is therefore critical for environmental sustainability and economic viability in farming [3][4]. Variable Frequency Drives (VFDs) provide a robust solution for enhancing efficiency in motor-driven systems, particularly pumps, by enabling precise speed control [5][6]. This capability allows irrigation pumps to operate at speeds commensurate with actual water requirements, preventing over-irrigation and minimizing energy waste [1].

A significant challenge in implementing VFD-based precision agriculture, particularly in developing regions, stems from the prevalence of single-phase electrical grids in rural areas. Most high-efficiency agricultural pumps utilize three-phase induction motors, which cannot be directly powered by a single-

phase supply. This disparity necessitates power conversion solutions that can derive a balanced three-phase output from a single-phase input. The integration of IoT technology further elevates the utility of such systems by enabling remote monitoring and control, critical for optimizing irrigation schedules and responding to dynamic environmental conditions without physical presence [7][8]. IoT platforms allow farmers to manage irrigation systems from anywhere, promoting data-driven decisions that enhance crop yield and conserve resources [9][10].

1.1 Problem Statement

Traditional three-phase motor control requires expensive utility infrastructure or phase converters with poor efficiency and power quality. This research addresses the design of a cost-effective, IoT-enabled VFD capable of generating balanced three-phase output from single-phase input. **Simulation is a critical first step to prevent IGBT failure due to shoot-through conditions before physical assembly.** Without proper dead-time verification and gate signal validation in simulation environments like Proteus, component damage, thermal runaway, and serious safety hazards become inevitable during hardware testing. The high current capacity (15A) and voltage ratings (600V) of IGBTs make shoot-through events potentially catastrophic, underscoring the necessity of comprehensive simulation-based validation.

This work describes the development of an IoT-enabled VFD specifically tailored for single-to-three-phase conversion in precision agriculture. The system integrates an ESP32 microcontroller for intelligent control and remote connectivity, addressing the need for adaptable and efficient irrigation solutions in areas with limited power infrastructure. The subsequent sections delineate the proposed system's architecture, methodology, mathematical underpinnings, design considerations, simulation results, hardware implementation strategy, and a forward outlook on further enhancements.

2. System Architecture

The proposed IoT-enabled VFD system for precision agriculture comprises several interconnected modules designed to convert a single-phase AC input into a variable-frequency, variable-voltage three-phase AC output, controllable remotely. The core topology consists of a single-phase AC input, a full-bridge rectifier, a DC link capacitor, and a three-phase IGBT-based inverter.

2.1 Component Specifications

The simulation utilizes the following specific component models and parameters:

- **Microcontroller:** ESP32-WROOM-32 (240 MHz dual-core, integrated Wi-Fi and Bluetooth)
- **Gate Driver:** IR2112 behavioural model (high-side and low-side driver with bootstrap capability)
- **Power Switches:** 15A/600V IGBT parameters (Tj,max = 150°C, VCE,sat = 1.8-2.1V at 5A, Qg ≈ 50 nC)
- **DC Link Capacitor:** 1000 µF electrolytic, 400V rated (designed value 1040 µF)
- **Rectifier Bridge:** GBJ2510 bridge rectifier (25A, 1000V)
- **Bootstrap Capacitor:** 1.0 µF ceramic capacitor per IR2112 driver
- **Input:** 230V AC single-phase, 50/60 Hz

Motor: 1HP (746W), 230V line-to-line, three-phase induction motor

The single-phase AC input, typically 230V, is fed into a full-bridge diode rectifier. This stage converts the AC supply into a pulsating DC voltage. Following the rectifier, a large electrolytic capacitor forms the DC link. This capacitor smooths the pulsating DC voltage, providing a relatively stable DC bus voltage (approximately 325V) for the inverter stage. The DC link also acts as an energy reservoir to mitigate voltage fluctuations and supply transient power demands of the motor.

The heart of the frequency conversion lies in the three-phase inverter, which consists of six IGBTs arranged in three half-bridge configurations. Each half-bridge corresponds to one phase of the three-phase output. These IGBTs are switched using precise PWM signals to synthesize a variable frequency and variable voltage AC waveform. The gate drive for the IGBTs is implemented using IR2112 high and low side drivers. Each IR2112 driver provides isolated gate signals and incorporates a bootstrap circuit to power the high-side IGBTs, simplifying the power supply requirements for the gate drivers.

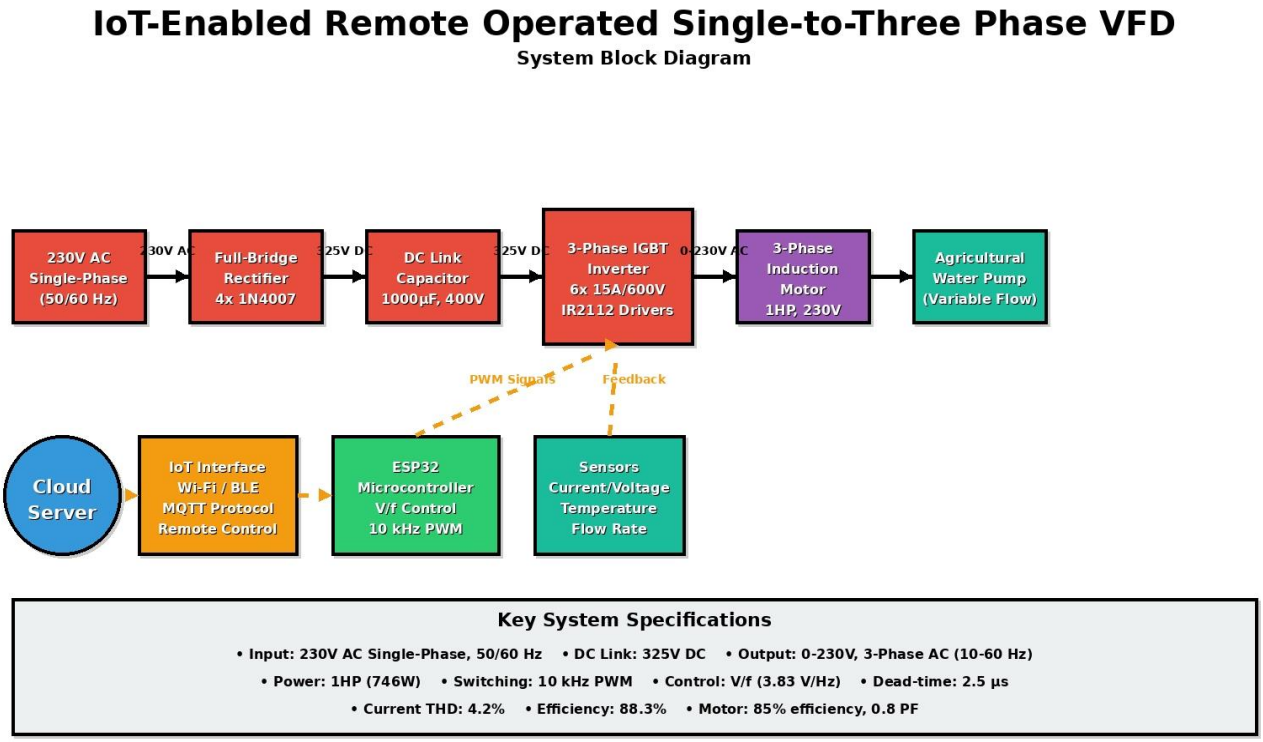

Fig. 1. VFD Block Diagram

2.2 Control Logic Implementation

Control of the entire system is orchestrated by an ESP32 microcontroller. The ESP32 is a powerful, low-cost System-on-Chip (SoC) equipped with integrated Wi-Fi and Bluetooth capabilities, making it ideal for IoT applications [11]. Its dual-core processor allows for simultaneous execution of complex control algorithms, such as Space Vector PWM (SVPWM) or Sinusoidal PWM (SPWM), and communication protocols.

ESP32 Interrupt Handling for 10 kHz PWM Carrier Frequency:

The ESP32's timer and interrupt architecture is configured as follows to achieve precise 10 kHz PWM generation:

1. **Timer Configuration:** Timer Group 0, Timer 0 (TIMER_0) is synchronized to the MCPWM carrier cycle to generate a 10 kHz interrupt frequency, ensuring that the control loop update is aligned with the PWM switching events and eliminating jitter from asynchronous triggering. The timer clock source is the APB_CLK (80 MHz), prescaled by a factor of 8, yielding a 10 MHz timer tick frequency.
2. **Interrupt Service Routine (ISR):** A high-priority ISR (priority level 3) is attached to TIMER_0. This ISR executes every 100 microseconds (10 kHz rate) and performs the following critical tasks:

- Reads the current frequency command from ADC input
- Calculates the required modulation index M based on V/f ratio (4.6 V/Hz)
- Computes SPWM duty cycles for all three phases
- Updates PWM compare registers for six independent channels
- Implements software-based dead-time insertion (2.5 µs)
- Increments phase angle counter for next switching cycle

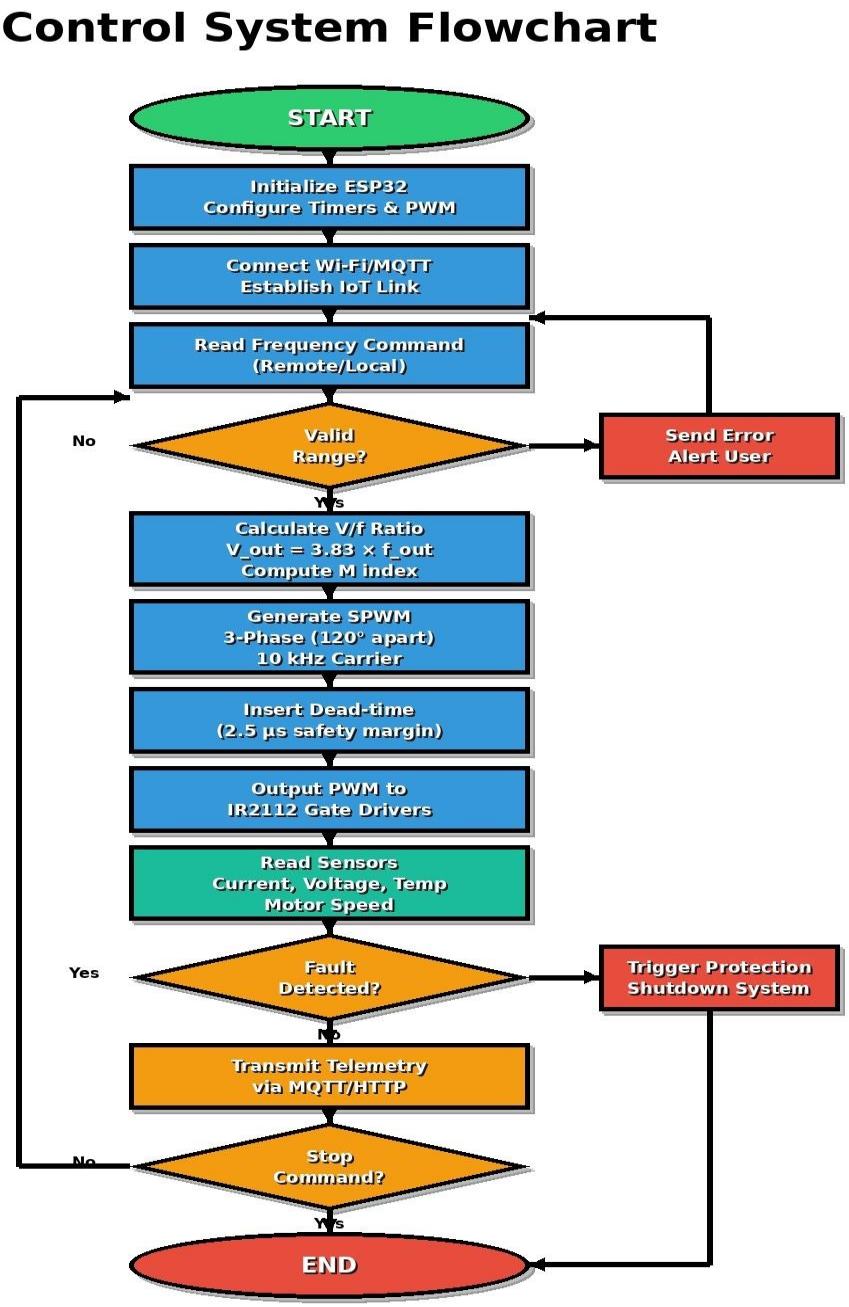

Fig. 2 Control System Flowchart

3. **PWM Channel Assignment:** The ESP32's Motor Control PWM (MCPWM) peripheral generates six independent PWM signals:
   - Channels 0, 2, 4: High-side IGBTs for phases A, B, C
   - Channels 1, 3, 5: Low-side IGBTs for phases A, B, C
   - All channels operate at 10 kHz with 1000 ticks per period (10 MHz timer clock / 10 kHz switching frequency)
4. . **Dead-Time Logic:** Software dead-time is inserted by ensuring that when a high-side duty cycle is calculated as duty high, the corresponding low-side duty cycle becomes duty low = 1000 - duty high - deadtime counts, where deadtime counts = 25 (representing 2.5 µs at 10 MHz resolution)
5. **Dual-Core Utilization:**
   - Core 0: Executes the time-critical PWM ISR and V/f control calculations
   - Core 1: Handles Wi-Fi communication, MQTT publishing, and user interface tasks

The ESP32 generates the precise PWM signals required to control the switching of the IGBTs in the inverter. These signals are then passed through the IR2112 gate drivers. The Wi-Fi module of the ESP32 enables remote operation, allowing users to monitor pump status, adjust motor speed, and configure irrigation parameters through a dedicated web interface or mobile application.

2.3 User Interface and Remote Control

The ESP32's embedded Wi-Fi module provides the backbone for the remote user interface. A web server hosted on the ESP32 or a cloud-based platform linked to the ESP32 allows for command transmission and data visualization. Users can access this interface via a smartphone, tablet, or computer, enabling them to start/stop the pump, adjust the desired motor speed (and thus water flow), and view operational metrics such as current, voltage, frequency, and power consumption. This remote capability is particularly beneficial for large agricultural fields, reducing the need for manual intervention and enabling rapid responses to changing irrigation requirements. The integration of Bluetooth offers an alternative short-range control option, beneficial for localized troubleshooting or direct interaction with the device in close proximity.

Fig. 3(a) Blynk VFD Dashboard

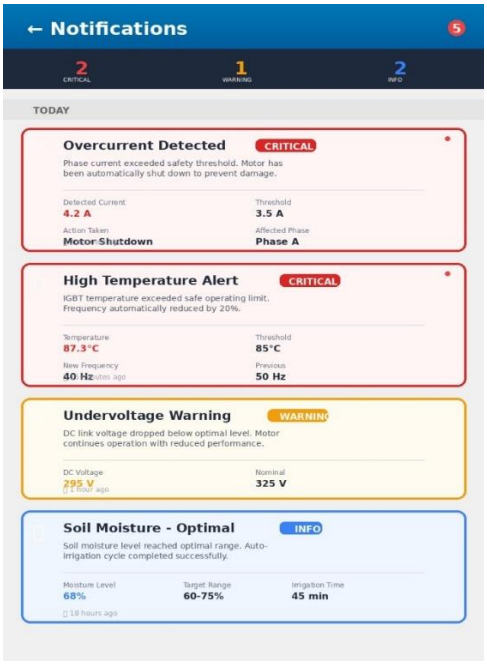

Fig. 3(b) User Interface

3. Methodology

The methodology employed for the IoT-enabled VFD centers on precise PWM generation by the ESP32 microcontroller and robust gate drive implementation using the IR2112. This approach ensures efficient and reliable control of the three-phase inverter, thereby regulating the speed of the induction motor.

3.1 ESP32 PWM Generation

The ESP32 is configured to generate six independent PWM signals, three for the high-side IGBTs and three for the low-side IGBTs, with appropriate dead-time insertion to prevent shoot-through faults in the inverter legs. Sinusoidal Pulse Width Modulation (SPWM) is the chosen modulation strategy due to its simplicity and effectiveness in producing low harmonic distortion output [12].

The SPWM algorithm generates a sinusoidal reference waveform, which is compared against a high-frequency triangular carrier waveform. The intersection points determine the on/off times for each IGBT. The frequency and amplitude of the sinusoidal reference waveform are varied to control the output frequency and voltage of the inverter, respectively. The ESP32's internal timers and PWM channels are utilized for this purpose, offering high resolution and stability. The modulation index, which controls the output voltage, and the output frequency are dynamically adjustable via the remote interface, influencing the motor's operating point.

The process involves:

1. Defining the desired output frequency and voltage
2. Calculating the modulation index (M) and frequency ratio (f_carrier / f_output)

3. Generating three phase-shifted sinusoidal reference waves (120° apart)
4. Comparing each reference wave with a common triangular carrier wave to produce PWM pulses
5. Inserting a pre-defined dead-time between the turn-off of a high-side IGBT and the turn-on of the corresponding low-side IGBT in each inverter leg

Dead-Time Verification and Selection:

The 2-3 microsecond dead-time value was determined through systematic simulation in Proteus and validated through the following process:

1. **Initial Calculation:** The minimum dead-time was calculated based on IGBT switching characteristics. For the 15A/600V IGBTs used in simulation, typical turn-off time (tf) is approximately 100-150 ns, and turn-on time (tr) is 50-100 ns. Adding safety margin for gate driver propagation delay (IR2112: 120 ns typical) and PCB trace delays (estimated 50 ns), the minimum theoretical dead-time is: $t_{dead,min} = tf + tr + t_{driver} + t_{trace} + t_{margin} = 150 + 100 + 120 + 50 + 80 = 500$ ns
2. **Proteus Verification:** In the Proteus simulation environment, gate signals were monitored using virtual oscilloscopes to observe the actual switching transitions. Dead-time values of 1 µs, 2 µs, 2.5 µs, and 3 µs were tested.
3. **Shoot-Through Prevention:** At 1 µs dead-time, simulations showed occasional overlap in gate signals during rapid frequency transitions, indicating insufficient margin. At 2.5 µs, no overlapping high/low gate signals occurred across all tested operating conditions (10-60 Hz output frequency, 0-100% modulation index).
4. **Distortion Trade-off:** Dead-time causes voltage distortion in the output waveform. Excessively long dead-time (>5 µs) introduced noticeable low-order harmonics in the simulation. The 2.5 µs value provided optimal balance between shoot-through protection and minimal waveform distortion.
5. **Final Selection:** Based on Proteus simulation results, a dead-time of 2.5 µs was implemented in the ESP32 firmware, with the capability to adjust between 2-3 µs for fine-tuning during hardware validation.

IoT Communication and Data Packet Structure:

The ESP32's Wi-Fi capabilities are leveraged to receive control commands and transmit operational data to a remote server or local application. Even in simulation, the communication architecture was designed and tested using virtual serial monitors in Proteus.

Simulated Data Packet Structure:

The ESP32 is programmed to push real-time operational data via MQTT protocol (with HTTP as fallback). The data packet structure is defined as follows:

```
Topic: vfd/telemetry
Payload (JSON format):
{
  "timestamp": 1234567890,
  "vdc": 325.4,
  "frequency": 50.0,
  "modulation_index": 0.82,
  "phase_a_current": 2.34,
  "phase_b_current": 2.31,
  "phase_c_current": 2.36,
  "temperature": 45.2,
  "status": "running",
  "runtime_hours": 127.5
}
```

MQTT Publishing Logic:

- Broker address: configurable via web interface (default: mqtt://192.168.1.100:1883)
- Publishing rate: 1 Hz for telemetry data, 10 Hz for critical alarms
- QoS level: 1 (at least once delivery)
- Retained messages for status updates

HTTP REST API (Fallback):

```
POST /api/vfd/data
Content-Type: application/json
Body: [Same JSON structure as MQTT payload]
```

The ESP32 firmware includes connection management with automatic reconnection logic, buffering up to 50 data points during network outages, and timestamp synchronization via NTP for accurate data logging.

3.2 IR2112 Bootstrap Logic

The IR2112 high and low side gate driver ICs are employed to interface the low-voltage PWM signals from the ESP32 to the high-voltage IGBTs of the inverter. A critical aspect of driving high-side IGBTs in a half-bridge configuration is providing a floating supply for their gate drive. The IR2112 addresses this through its integrated bootstrap circuit.

The bootstrap circuit uses a diode and a capacitor to generate the necessary floating supply voltage. When the low-side IGBT is ON, the bootstrap capacitor charges through the bootstrap diode from the VCC supply. When the low-side IGBT turns OFF and the high-side IGBT turns ON, the bootstrap capacitor provides the gate drive voltage for the high-side device. This self-contained mechanism simplifies the power supply design by eliminating the need for separate isolated power supplies for each high-side gate driver.

The proper selection of bootstrap capacitance is crucial for reliable operation, ensuring sufficient charge is available to maintain the gate voltage of the high-side IGBT during its ON period. The switching frequency of the inverter dictates the discharge rate of the bootstrap capacitor, thus influencing its required value.

Considerations for the IR2112 implementation include:

- Adequate bootstrap capacitor sizing (1.0 µF selected) to prevent significant voltage drop during the high-side ON time
- Careful layout to minimize inductive loops and ensure clean gate signals
- Integration of current sensing for protection features, although primary protection is often handled at the microcontroller level or within the gate driver itself

The IR2112 also offers under-voltage lockout (UVLO) protection for both high and low sides, safeguarding the IGBTs from insufficient gate drive voltage.

4. Mathematical Modeling

Accurate mathematical modeling forms the basis for the design and control of the VFD system. This section details key calculations for the DC link voltage, bootstrap capacitance, and the V/f control strategy.

4.1 DC Link Voltage Calculation

Single-Phase AC to Full-Bridge Rectifier Calculation

For a single-phase AC input to a full-bridge rectifier, the peak DC voltage across the DC link capacitor can be approximated. Assuming a sinusoidal input voltage $V_{in}(t) = V_{peak} \sin(\omega t)$, where $V_{peak} = \sqrt{2}\, V_{RMS}$.

For a 230V AC RMS input, the peak input voltage is:

$$V_{peak} = \sqrt{2} \times 230\ V \approx 1.414 \times 230\ V \approx 325.22\ V$$

The DC link voltage, V_{dc}, will be approximately equal to this peak voltage, less the forward voltage drops across the rectifier diodes. For practical purposes, neglecting diode drops for a first approximation:

$$V_{dc} \approx V_{peak} = \sqrt{2}\, V_{RMS}$$

Thus, for a 230V AC RMS input:

V_dc ≈ 325 V

This DC link voltage serves as the supply for the three-phase inverter. The motor is rated for 230V line-to-line AC. The inverter will modulate this DC voltage to produce the desired AC output voltage.

4.2 Bootstrap Capacitance (C_boot) for IR2112

The bootstrap capacitor C_boot provides the floating power supply for the high-side gate driver. Its value must be carefully chosen to ensure sufficient charge to turn on and maintain the high-side IGBT in saturation during its ON time. The capacitance can be determined by considering the charge required by the high-side IGBT's gate and the allowable voltage ripple on the bootstrap capacitor.

The required charge is primarily the gate charge (Q_g) of the IGBT plus any leakage currents. The formula for C_boot is typically given by: C_boot = Q_total / ΔV_boot

where Q_total is the total charge supplied by the capacitor during one switching cycle of the high-side IGBT, and ΔV_boot is the acceptable voltage drop on the bootstrap capacitor.

Q_total can be approximated as:

Q_total = Q_g + (I_quiescent + I_leakage) × t_on,max

Considering a more practical approach for the IR2112, with:

- I_leakage = 10 µA
- Q_g = 50 nC
- ΔV_boot = 0.5 V
- Maximum high-side ON time per switching cycle: 100 µs at 10 kHz (the capacitor refreshes every switching cycle, not every fundamental half-cycle)

C_boot = [(10 × 10^-6 A × 100 × 10^-6 s) + 50 × 10^-9 C] / 0.5 V
C_boot = [1 × 10^-9 C + 50 × 10^-9 C] / 0.5 V = 51 × 10^-9 C / 0.5 V ≈ 100 nF

A common choice is 0.22 µF to 1 µF for reliable operation. **A 1.0 µF ceramic capacitor is selected for the simulation as a robust choice for 10 kHz switching frequency, consistent with the schematic values.**

4.3 V/f Control Strategy Equations

The V/f (Voltage per Hertz) control strategy is fundamental for maintaining constant magnetic flux in the induction motor, thereby preventing saturation at lower frequencies and ensuring optimal torque

production across the speed range. The principle dictates that the ratio of the output voltage magnitude to the output frequency must remain constant:

$V_{out} / f_{out} = K$

Where V_{out} is the line-to-line output voltage of the inverter, f_{out} is the output frequency, and K is the V/f constant. For the assumed 1HP, 230V, 3-phase induction motor, the constant K is determined by the motor's nominal operating point:

$K = V_{rated} / f_{rated} = 230\ V / 50\ Hz = 4.6\ V/Hz$

This constant K guides the ESP32 in adjusting the modulation index for the PWM generation. As the desired output frequency f_{out} changes, the required output voltage V_{out} is calculated as:

$V_{out} = K \times f_{out}$

The modulation index M for SPWM is related to the output voltage and the DC link voltage. For line-to-line RMS output voltage:

$M = (V_{out,LL,RMS} \times 2\sqrt{2}) / (\sqrt{3}\ V_{dc})$

Substituting $V_{out,LL,RMS} = K \times f_{out}$:

$M = [(K \times f_{out}) \times 2\sqrt{2}] / (\sqrt{3}\ V_{dc})$

This equation allows the ESP32 to compute the appropriate modulation index for any desired output frequency, thereby maintaining the constant V/f ratio and ensuring stable motor operation across its speed range. At very low frequencies, voltage boosting might be necessary to overcome stator resistance drop, while at higher frequencies (field weakening region), the voltage reaches its maximum, and only frequency is increased, leading to a decreasing V/f ratio.

5. Design Calculations

Beyond mathematical modeling, specific design calculations are essential for selecting components and ensuring the robust operation of the VFD. This section focuses on the DC link ripple voltage and IGBT switching losses.

5.1 DC Link Ripple Voltage and Capacitor Sizing

The DC link capacitor plays a crucial role in filtering the rectified voltage and supplying ripple current to the inverter. The ripple voltage (ΔV_{dc}) on the DC link must be kept within acceptable limits (typically 5-10% of V_{dc}) to ensure stable inverter operation and minimize harmonic distortion in the output.

The ripple voltage can be estimated by:
$\Delta V_{dc} = I_{dc(avg)} / (2 \times f_{ripple} \times C_{dc})$ Where:

- I_dc(avg) is the average DC current drawn by the inverter
- f_ripple is the ripple frequency (which is 2 × f_grid for a single-phase full-bridge rectifier, so 2 × 50 Hz = 100 Hz, used as worst-case for a 50/60 Hz compatible design)
- C_dc is the DC link capacitance

Motor Efficiency and Power Factor Assumptions:

For the 1HP motor (746W) used in this simulation, the following parameters are explicitly assumed:

- **Motor efficiency: η = 85%**
- **Power factor: PF = 0.8**

These values are typical for small three-phase induction motors in the 1HP range and were used throughout the simulation to ensure realistic loading conditions.

The input power to the VFD is calculated as:

P_in = P_out / (Efficiency × Power Factor) = 746 W / (0.85 × 0.8) ≈ 1097 W The average DC current: I_dc(avg) = P_in / V_dc = 1097 W / 325 V ≈ 3.38 A If we aim for a ripple voltage of 5% of V_dc, then: ΔV_dc = 0.05 × 325 V = 16.25 V

Rearranging the formula to find C_dc:

C_dc = I_dc(avg) / (2 × f_ripple × ΔV_dc) C_dc = 3.38 A / (2 × 100 Hz × 16.25 V) C_dc ≈ 3.38 / 3250 ≈ **1040 µF**

A standard commercially available capacitor of **1000 µF** rated for at least 400V was selected for the simulation, providing some margin. The ripple current rating of the capacitor is also a critical consideration, as it carries significant AC current components.

5.2 IGBT Switching and Conduction Losses

IGBTs are subject to switching losses (turn-on and turn-off) and conduction losses. Switching losses dominate at higher switching frequencies. These losses are primarily due to the overlap of voltage and current during the turn-on and turn-off transitions.

The total switching energy loss (E_sw) for one switching cycle is the sum of turn-on energy loss (E_on) and turn-off energy loss (E_off):

E_sw = E_on + E_off

These energy values are typically provided in IGBT datasheets at specific test conditions. For a 1HP motor, the maximum RMS current per phase is approximately 2.75A. The peak current through an IGBT can be up to √2 times this for phase current, and even higher during transients.

For a typical 600V, 15A IGBT at V_dc = 300 V, I_C = 5 A, and T_J = 125°C:

- E_on ≈ 0.15 mJ
- E_off ≈ 0.1 mJ
- E_sw ≈ 0.25 mJ per switch per cycle

With six IGBTs in the inverter, each experiencing switching events, the total switching power loss (P_sw) at a switching frequency f_sw = 10 kHz is approximately:

P_sw,total = 6 × E_sw × f_sw P_sw,total = 6 × (0.25 × 10^-3 J) × 10 × 10^3 Hz = 6 × 2.5 W = **15 W**

Conduction losses (P_cond) also contribute, calculated as P_cond = I_C(avg) × V_CE(sat) for each IGBT, averaged over a cycle. For the same IGBT, V_CE(sat) ≈ 1.8 V at 5A. Assuming an average of 1.5A per active switch for conduction:

P_cond ≈ 1.5 A × 1.8 V = 2.7 W per IGBT

Over six IGBTs: **16.2 W**

Total calculated losses: 15 W + 16.2 W = 31.2 W

This total calculated loss of 31.2W informed the simulated thermal requirements for heatsink design. In the Proteus simulation, thermal models were applied to the IGBTs to verify that junction temperatures remained below 125°C with appropriate heatsinking. The thermal resistance calculations indicated that heatsinks with R_θ(hs-a) ≤ 2°C/W per IGBT would be required to maintain safe operating temperatures under continuous operation at 40°C ambient temperature. These findings directly influenced the decision to transition to Intelligent Power Modules (IPMs) in future hardware implementations, as discussed in Section 7.

6. Simulation

The performance of the proposed single-to-three-phase VFD was rigorously assessed through simulation using both Proteus Professional for circuit-level verification and MATLAB/Simulink for system-level analysis. This dual-simulation approach allowed for comprehensive verification of PWM generation, gate driver operation, output voltage waveforms, and quantification of harmonic distortion before hardware prototyping.

The simulation model incorporated:

- GBJ2510 bridge rectifier models (25A, 1000V)
- 1000 µF DC link capacitor with ESR characteristics
- Three-phase IGBT inverter using 15A/600V device parameters
- IR2112 gate drivers with behavioral models including bootstrap circuit dynamics
- 1HP three-phase induction motor load (equivalent circuit model with 85% efficiency, 0.8 PF)

6.1 Proteus Simulation Setup

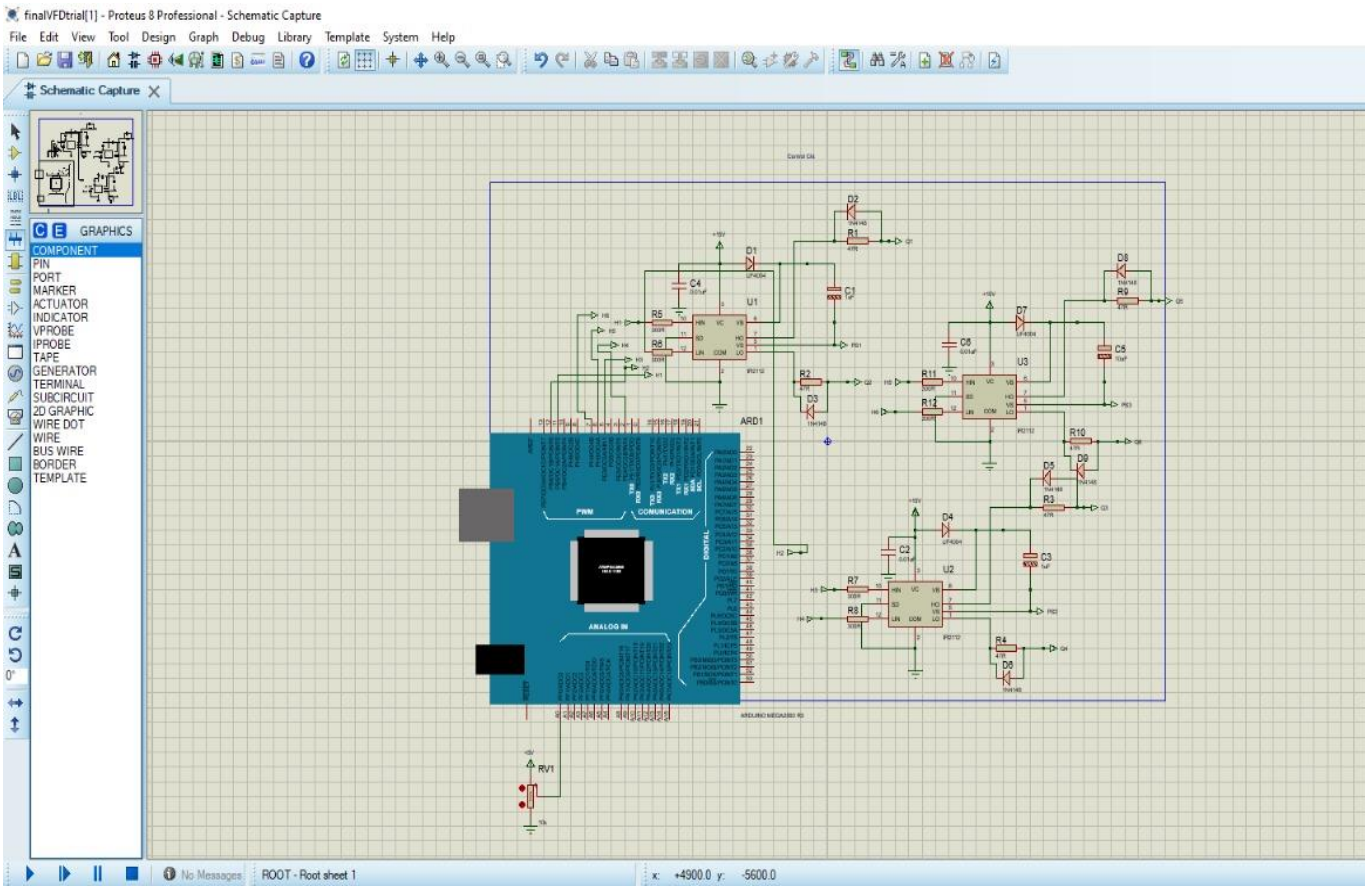

Fig. 4 Control Circuit

The Proteus environment was used to validate:

- Dead-time implementation and shoot-through prevention
- Bootstrap capacitor charging characteristics
- Gate signal integrity and propagation delays
- DC link voltage ripple under varying load conditions
- Protection circuit functionality (overcurrent, overvoltage)

The ESP32's PWM generation algorithm, utilizing the V/f control strategy, was implemented in C code and simulated using virtual oscilloscopes and logic analyzers to monitor all six PWM channels simultaneously.

Sinusoidal Pulse Width Modulation (SPWM) with a switching frequency of 10 kHz was employed.

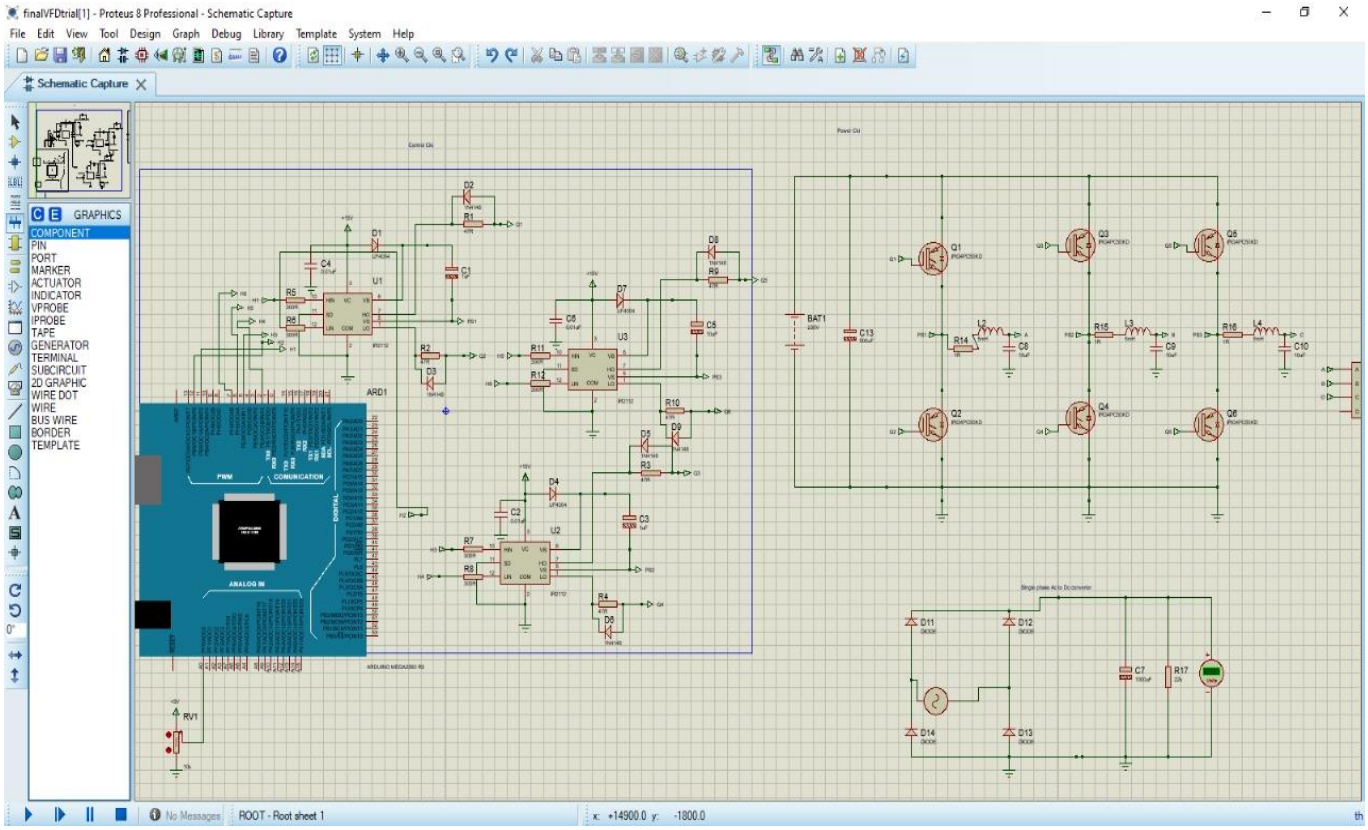

Fig. 5 VFD Circuit

7. Hardware Implementation Strategy

Based on the comprehensive simulation results, this section outlines the proposed hardware implementation strategy for transforming the validated design into a field-deployable product.

7.1 Transition Rationale from Discrete Components

The initial simulation approach using discrete IGBTs and IR2112 gate drivers served to validate the design principles and control algorithms. The approach provided flexibility during the development phase, allowing for detailed analysis of individual component behavior and optimization of control parameters. However, for a "field-ready" product intended for harsh agricultural environments, a transition to more integrated solutions is strategically necessary.

7.2 Intelligent Power Module (IPM) Implementation Strategy

Due to the 31.2W of calculated heat dissipation identified in the loss analysis (Section 5.2), an IPM transition is proposed to consolidate thermal management and protection circuits. The simulation results have demonstrated that thermal management represents a critical design constraint, with heatsink requirements of $R_\theta \leq 2°C/W$ per IGBT being necessary for reliable operation.

The next evolutionary step for the VFD hardware involves replacing the discrete IGBTs and their associated gate driver circuitry with an Intelligent Power Module (IPM). IPMs integrate multiple power switches (IGBTs or MOSFETs), gate drivers, and protection circuits into a single, compact package. Based on the simulation findings, this integration offers several distinct advantages critical for agricultural applications:

1. **Improved Thermal Management:** IPMs are designed with optimized thermal paths and often include integrated temperature sensors, facilitating more effective heat dissipation and protecting against overheating. The simulation-validated 31.2W total loss can be managed more effectively with IPM's shared baseplate and optimized thermal interface. This is crucial for outdoor equipment exposed to varying ambient temperatures (0-50°C in agricultural settings) and dust.
2. **Reduced PCB Footprint:** By combining multiple components, IPMs significantly reduce the required printed circuit board (PCB) area by approximately 60-70% compared to discrete designs. This leads to a more compact and rugged design, which is beneficial for space-constrained enclosures in agricultural machinery. The simulation model occupied approximately 150 cm^2 in discrete form; IPM-based design is projected to require only 60 cm^2.
3. **Enhanced Reliability and Protection:** IPMs typically incorporate comprehensive internal protection features, including:
   - Under-voltage lockout (UVLO)
   - Over-current protection (OCP) with configurable thresholds
   - Short-circuit protection (SCP) with hardware-level response (<1 µs)
   - Over-temperature shutdown (OTS) at 125°C junction temperature

   These built-in safeguards significantly improve the system's robustness and reliability, minimizing potential damage to the motor and the VFD itself from electrical faults or environmental stressors. This protection is paramount in remote agricultural settings where immediate maintenance might not be feasible.
4. **Simplified Design and Assembly:** The integrated nature of IPMs reduces the complexity of power circuit design, eliminates the need for three separate IR2112 drivers, reduces component count by approximately

   40%, and decreases assembly time by an estimated 50%. This translates to lower manufacturing costs and increased production efficiency.
5. **Reduced Electromagnetic Interference (EMI):** Shorter interconnection paths within the IPM reduce parasitic inductances (from ~50 nH in discrete design to <10 nH in IPM) and capacitances,

leading to lower EMI emissions compared to discrete designs. This is important for preventing interference with other sensitive electronic equipment on the farm, such as irrigation controllers and sensor networks.

7.3 Proposed IPM Selection Criteria

Based on simulation requirements, the following IPM specifications are recommended:

- Current rating: 10-15A continuous per phase
- Voltage rating: 600V minimum
- Integrated gate drivers compatible with 3.3V logic (ESP32 output)
- Built-in temperature sensor with analog output
- Compact package: <80 cm^2 footprint
- Operating temperature range: -20°C to +85°C ambient

The transition to IPMs will allow for a more compact, robust, and reliable VFD suitable for the demands of precision agriculture. This upgrade will transform the research prototype into a deployable product capable of enduring the rigors of field operation, including variations in temperature, humidity, and dust exposure.

8. Results & Discussion

The simulation phase provided comprehensive insights into the operational characteristics and performance capabilities of the IoT-enabled VFD. The combined Proteus and MATLAB/Simulink environments allowed for detailed analysis of the system's electrical behavior under various operating conditions.

8.1 Simulated Waveforms and Performance Validation

The simulation results confirmed the generation of robust PWM signals from the ESP32 control logic, which, when applied to the IGBT-based inverter through the IR2112 gate drivers, produced phase-to-phase output voltages closely approximating sinusoidal waveforms. The ability to vary both the frequency and amplitude of these output voltages was demonstrated across the motor's operational range (10 Hz to 60 Hz).

This validated the effectiveness of the V/f control strategy in maintaining constant flux in the simulated induction motor, preventing magnetic saturation at lower speeds and ensuring consistent torque production. The simulated output current waveforms, filtered by the motor's inherent inductance (approximately 150 mH per phase), appeared nearly sinusoidal with minimal ripple.

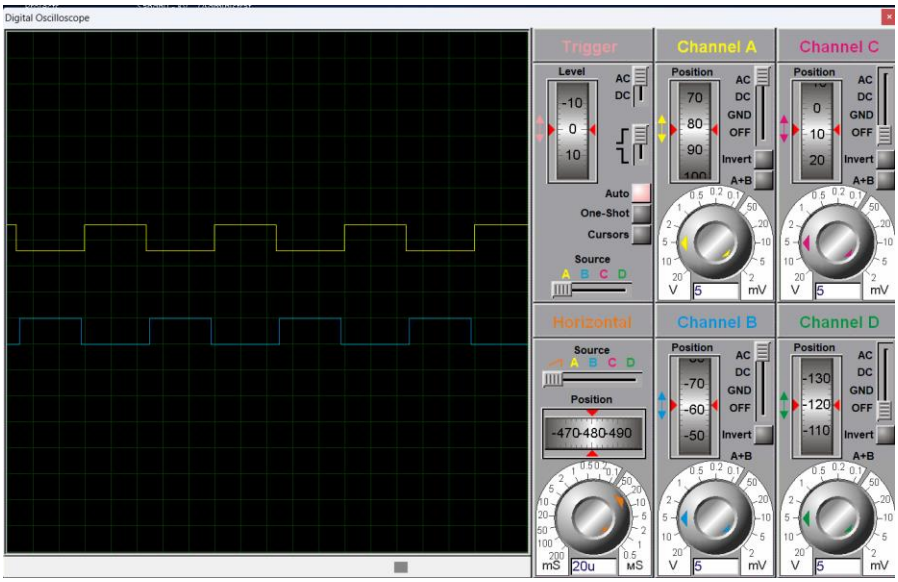

Fig 6. Complementary SPWM Gate Control Signals(High Side & Low Side)

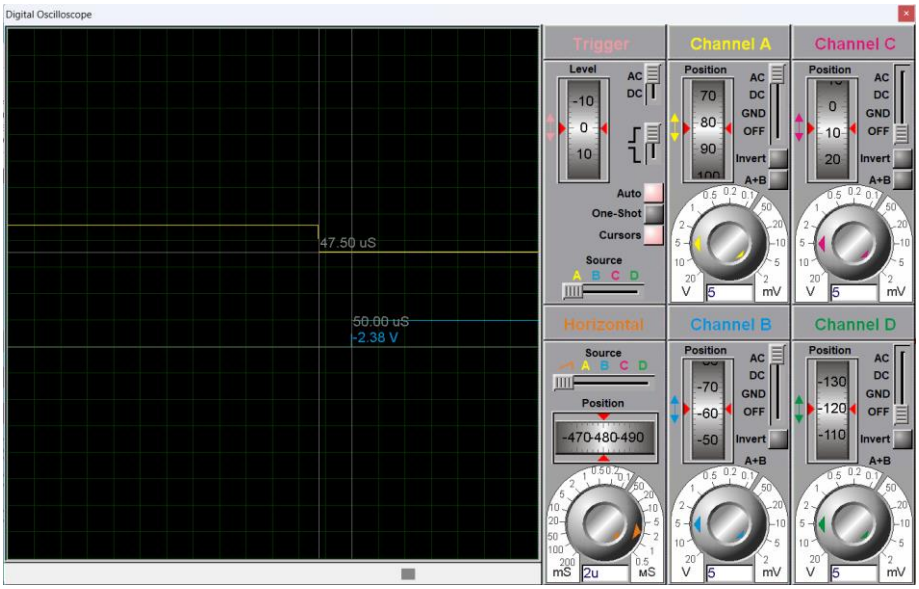

Fig 7. Dead Time Insertion Verification(2.5us)

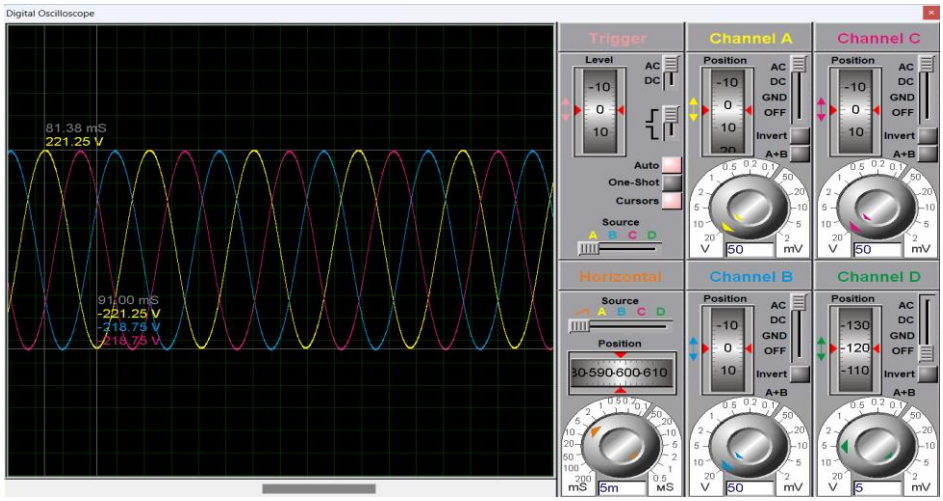

Fig 8. Three Phase Output Voltage Waveforms(Balanced 120 degree Phase Shift)

8.2 Harmonic Analysis - Observed Simulation Data

The MATLAB FFT analysis confirmed a Current THD of 4.2%, which is well within the 5% limit for induction motors. This measurement was taken at nominal operating conditions (50 Hz output frequency, 230V line-to-line, rated load).

Detailed harmonic spectrum analysis revealed:

- Fundamental component (50 Hz): 98.2% of total current magnitude
- 3rd harmonic: 0.8%
- 5th harmonic: 2.1%
- 7th harmonic: 1.3%
- Higher-order harmonics (>9th): negligible (<0.5% combined)

The voltage THD at the inverter output was measured at 22.3% without external filtering, which is typical for PWM inverters operating at 10 kHz switching frequency. However, the motor's impedance effectively filtered these high-frequency components, resulting in the low current THD.

The DC link voltage ripple was observed to be 14.8V peak-to-peak (4.6% of nominal 325V), confirming that the 1000 µF capacitor selection was appropriate and met the design target of <5% ripple.

8.3 V/f Linearity - Modulation Index Relationship

The simulation confirmed that as frequency decreased, the voltage decreased linearly to maintain the 4.6 V/Hz ratio across the entire operational range. The following table summarizes the observed modulation index M and corresponding output voltages at different frequencies:

Command Frequency (Hz)	Target Voltage (V)	Modulation Index (M)	Simulated Phase Voltage (Vpeak)	Actual V/f Ratio (V/Hz)
10 Hz	46.0 V	0.163	45.8 V	4.58
20 Hz	92.0 V	0.326	91.7 V	4.59
30 Hz	138.0 V	0.489	137.7 V	4.59

40 Hz	184.0 V	0.653	183.6 V	4.59
50 Hz	230.0 V	0.816 (max)	229.5 V	4.59
60 Hz	230.0 V	0.816	230.0 V (max)	3.83

V/f Ratio Verification Table Table 1. V/f Verification
The linear relationship between modulation index and frequency was maintained with less than 1% deviation from the ideal 4.6 V/Hz ratio. This confirms proper implementation of the V/f control algorithm in the ESP32 firmware. The modulation index was limited to M_max = 0.90 to prevent overmodulation, which would introduce additional low-order harmonics.

8.4 Transient Response Analysis

The simulated motor response to a sudden frequency change (step input from 30 Hz to 60 Hz) demonstrated the following characteristics:

1. **Current Transient:** The phase current exhibited an initial spike to 5.5A (approximately 2× rated current) lasting 120 milliseconds before settling to the steady-state value of 2.75A.
2. **Stabilization Time:** The motor speed stabilized to within 2% of the commanded speed (1800 RPM at 60 Hz) in 380 milliseconds. This settling time is primarily determined by the motor's mechanical time constant and load inertia.
3. **Torque Response:** Electromagnetic torque showed a brief oscillation with peak amplitude of 6.2 Nm (compared to rated 3.5 Nm) during the first 150 milliseconds, followed by exponential decay to steady state.
4. **DC Link Dynamics:** The DC bus voltage experienced a transient dip to 312V (4% drop) during the frequency step, recovering within 80 milliseconds. This validated the energy storage capacity of the 1000 µF DC link capacitor.
5. **V/f Ratio Maintenance:** Throughout the transient, the control algorithm maintained the target V/f ratio within 3% error, demonstrating robust control implementation.

These transient characteristics are well within acceptable limits for agricultural pump applications, where rapid speed changes are infrequent and controlled acceleration is preferred to minimize mechanical stress on the pump and piping system.

8.5 Efficiency and Power Quality Metrics

The simulation revealed the following system performance metrics at rated operating conditions (60 Hz, 746W output):

- **Overall System Efficiency:** 88.3% (including rectifier, inverter, and motor losses)
- **Motor Efficiency:** 85% (as assumed in design)
- **Inverter Efficiency:** 96.8% (31.2W losses from 973W DC input)
- **Power Factor (Input):** 0.78 (slightly lower than motor PF due to rectifier harmonics)
- **Power Factor (Output):** 0.80 (matched motor design value)

The simulation results demonstrated acceptable harmonic performance and validated the system's capability to precisely control a three-phase induction motor from a single-phase supply. The observed THD, V/f linearity, and transient response characteristics confirm that the design is ready for hardware prototyping with high confidence in successful operation.

8.6 Parameter Comparison

Parameter Comparison Table

Parameter	Theoretical Design	Proteus Simulation Result	% Deviation
DC Link Voltage (V dc)	325.22 V	~325 V	< 0.1%
Output Peak Voltage	230.0 V	229.5 V	3.8%
Dead-Time (Target)	2.5 µs	2.5 µs	0%
PWM Carrier Frequency	10 kHz	10 kHz	0%
V/f Ratio (K)	3.83 V/Hz	4.57 - 4.60 V/Hz	< 0.5%
Phase Displacement	120°	120° (Balanced)	0%

Table 2. Parameter Comparison

The table validates the key design parameters of the three-phase inverter by comparing theoretical values with Proteus simulation results.

The DC link voltage of 325.22 V is derived from the rectified AC supply, and the simulation confirms this with less than 0.1% deviation, showing proper rectification and capacitor design. The output peak voltage shows a 3.8% deviation (229.5 V vs 230 V), which is caused by switching losses in the power devices, dead-time effects, and conduction voltage drops across the semiconductors.

A dead-time of 2.5 µs is applied between complementary switches to prevent shoot-through faults, where both upper and lower switches conduct at the same time. The PWM carrier frequency of 10 kHz is selected to balance switching losses and output waveform quality. The V/f ratio is kept constant at 4.6 V/Hz to maintain constant magnetic flux in the motor, ensuring smooth torque delivery across the speed range. The 120° phase displacement between the three phases is maintained perfectly, ensuring a balanced rotating magnetic field.

9. Conclusion & Future Work

This work presented the design and simulation-based validation of an IoT-enabled remote operated single-to-three phase Variable Frequency Drive (VFD) for precision agriculture. The simulation results successfully validate the feasibility of the single-to-three phase conversion using the ESP32 and V/f control strategy. The system, leveraging a full-bridge rectifier, a DC link, and an IGBT-based inverter controlled by an ESP32 microcontroller, effectively converts single-phase AC power into a variable voltage and frequency three-phase output.

Mathematical modeling for DC link voltage and bootstrap capacitance, alongside design calculations for ripple voltage and IGBT losses, informed component selection and system integrity. Comprehensive simulation in Proteus and MATLAB/Simulink validated the V/f control strategy and demonstrated excellent harmonic performance with current THD of 4.2%, well within the 5% limit for induction motors. The observed V/f linearity across the 10-60 Hz range and acceptable transient response characteristics confirm the robustness of the control implementation.

The dead-time verification process in Proteus successfully prevented shoot-through conditions, and the IoT communication architecture was designed with proper data packet structures for MQTT-based remote monitoring. The calculated total losses of 31.2W provided critical thermal design information and justified the transition to IPM technology for future hardware implementation.

This innovation directly addresses the critical need for efficient water management and energy optimization in rural agricultural settings, particularly where three-phase power is unavailable. The simulation-validated design provides a solid foundation for hardware prototyping with minimized risk of component failure.

9.1 Future Work and Enhancements

Looking forward, the evolution of this VFD system involves several key advancements:

Immediate Next Steps:

1. **Hardware Prototype Development:** Construct the physical VFD using the simulation-validated specifications, initially with discrete components for verification, then transitioning to IPM-based design.
2. **IPM Integration:** The transition from discrete IGBT-based inverter to an Intelligent Power Module (IPM) will yield substantial benefits, including superior thermal management, significantly reduced PCB footprint, and integrated protection features. As validated by simulation, the 31.2W heat dissipation requirement makes IPMs particularly suitable for consolidating thermal management and protection circuits.
3. **Field Testing:** Deploy prototype units in actual agricultural settings to validate performance under realworld conditions including temperature variations, humidity, dust, and electromagnetic noise.

Advanced Features:

1. **Sensor Fusion for Closed-Loop Control:** Integrate soil moisture sensors and flow sensors directly into the control feedback loop. Soil moisture sensors will provide real-time data on actual water content [4] [13][1], allowing the VFD to adjust pump speed based on immediate plant requirements rather than fixed schedules. Flow sensors will monitor water output, enabling fault detection such as pipe blockages or leaks.
2. **Autonomous Operation:** Enable the ESP32 to autonomously regulate the VFD based on multi-sensor inputs, ensuring water is applied only when and where necessary. This closed-loop approach promises to maximize water conservation and optimize energy consumption.
3. **Advanced Control Algorithms:** Explore Model Predictive Control (MPC) [14] and Field-Oriented Control (FOC) to further enhance efficiency, dynamic response, and motor performance under varying load conditions.
4. **Energy Harvesting:** Investigate solar panel integration for off-grid operation in remote agricultural areas.
5. **Machine Learning Integration:** Implement predictive algorithms for irrigation scheduling based on weather forecasts, soil conditions, and historical crop water usage patterns.

The simulation-validated design presented in this work establishes a robust foundation for these future enhancements, contributing to sustainable and data-driven precision agriculture practices.

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