Advanced International Journal for Research (AIJFR)
E-ISSN: 3048-7641 ● Website: www.aijfr.com ● Email: editor@aijfr.com

Power Quality improvement by Diode Clamped Multievel Inverter

Dr.Rashmy Deepak[1], Vijaylaksmi M. S[2], Likhitha G. Basavaraju[3]

[1]Assitant Professor
[1]Department of Electrical & Electronics RNS Institute of Technology Bengaluru, India
[2,3]Department of Electrical & Electronics
RNS Institute of Technology Bengaluru, India

Abstract

Multilevel inverters, particularly diode-clamped topologies, have emerged as effective solutions for enhancing power quality in modern power systems, including renewable energy integration and grid-connected applications. This paper investigates the performance of a 7-level diode-clamped multilevel inverter (DCMLI) for power quality improvement, focusing on harmonic reduction and voltage waveform enhancement through advanced pulse width modulation (PWM) techniques. A comprehensive simulation study using MATLAB/Simulink evaluates Sinusoidal PWM (SPWM) with various carrier disposition schemes. Results demonstrate that Modified SVPWM with Phase Disposition (PD) and trapezoidal carriers achieves the lowest Total Harmonic Distortion (THD) of 7.35% for phase voltage, alongside 15–16% improved DC link utilization compared to conventional SPWM. Experimental validation on a 400 V prototype confirms these findings, with THD reduced to 7.98%.

Keywords— Power Quality, Diode-Clamped Multilevel Inverter, Sinusoidal PWM, Switching Losses, Multi-level Topology, Voltage Balancing

1. INTRODUCTION

Power quality issues, such as harmonic distortion, voltage sags, and neutral-point imbalance, pose significant challenges in electrical distribution systems, particularly with the proliferation of nonlinear loads and renewable energy sources. Traditional two-level inverters exacerbate these problems due to high dv/dt and switching losses. Multilevel inverters (MLIs) address these limitations by synthesizing output voltages with multiple discrete levels, approximating a sinusoidal waveform and thereby reducing harmonics without increasing switching frequency. Among MLI topologies, the diode-clamped multilevel inverter (DCMLI), also known as neutral-point-clamped (NPC), offers robustness and simplicity in clamping voltage stresses using diodes[2]. For a 7-level DCMLI, the output voltage steps are generated from a divided DC bus, enabling applications in medium-voltage drives and photovoltaic systems. This paper focuses on power quality enhancement via a 7-level DCMLI, employing modified PWM strategies to minimize THD and optimize DC utilization[3]. The structure is motivated by recent advancements in PWM for MLIs, where selective harmonic elimination and carrier-based techniques reduce computational complexity while improving output quality. In a 7-level diode-clamped multilevel

inverter, the DC-link voltage is divided into multiple segments using capacitors, enabling the generation of seven distinct voltage levels at the output. Increasing the number of voltage levels results in a further reduction of lower-order harmonics and improved voltage waveform quality compared to lower-level configurations [5**]**. Consequently, the need for bulky passive filters is minimized, contributing to compact and cost-effective system design.

Recent developments in pulse-width modulation (PWM) techniques have further enhanced the performance of multilevel inverters. Advanced carrier-based modulation and selective harmonic elimination strategies allow effective control of switching states while reducing computational complexity and improving DC bus utilization **[**4], [6**]**. These modulation methods play a crucial role in minimizing total harmonic distortion (THD) and maintaining capacitor voltage balance in diode-clamped inverters.

This paper focuses on power quality improvement using a 7-level diode-clamped multilevel inverter. The study emphasizes harmonic reduction and voltage waveform enhancement through appropriate inverter configuration and modulation strategy. Simulation-based analysis is presented to demonstrate the effectiveness of the proposed approach, highlighting its suitability for modern power quality–oriented applications in industrial and renewable energy systems.

2. DCMLI TOPOLOGY

- Diode Clamped MLI[1]
- Cascaded H-Bridge MLI[7][8]
- Flying Capacitor MLI[9]

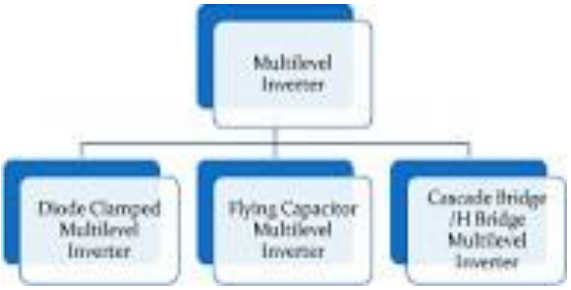

Fig.1- Different topologies of Multilevel Inverter

3. DIODE- CLAMPED MULTILEVEL INVETER

The basic structure of diode clamped MLI is composed of two voltage source inverters by connecting positive terminal of a VSI module to negative of another module and producing an another level. To make a neutral point 'N', clamping diodes are used and each semiconductor device has to block half of inverter voltage [4].

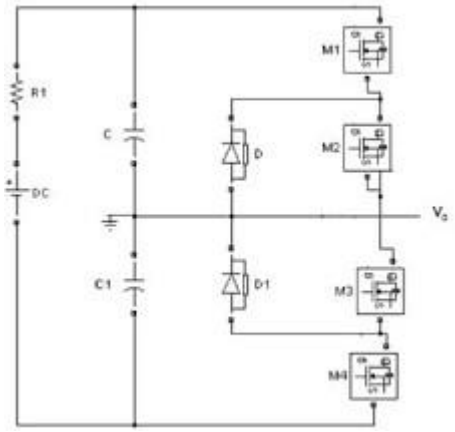

Fig.2- Three level diode clamped MLI

The output voltage is expressed as where N is chosen as the neutral point. The series connecting bulk capacitors Cdc can split the DC bus voltage Vdc into three levels[3]. The switching state for different output is shown as follows:

- When the output voltage VAN = Vdc / 2, the upper two switch S1 and S2 are closed.
- When van = 0, the switch S2 and S3 are closed.
- When van = −Vdc/ 2, the lower two switch S3 and S4 are closed.

"The three-level inverter is discussed for conceptual understanding, while the proposed system focuses on a seven-level DCMLI."

CIRCUIT CONFIGURATION OF THE 7-LEVEL DIODE-CLAMPED INVERTER FUNCTION AND OUTPUT

- Voltage Stress Limitation: The clamping diodes limit the maximum voltage stress across any single switch to Vdc/3, 2Vdc/3, and Vdc allowing lower-voltage-rated components with better switching characteristics.[6]
- Voltage Level Synthesis: By selectively turning on/off the 12 switches, the output terminal can connect to four positive and four negative voltage nodes (including the DC negative terminal).
- Output Voltage Level:
  The phase voltage of the 7-level diode-clamped multilevel inverter synthesizes seven discrete

voltage levels given by: $V_{phase} \in \{-Vdc, -2Vdc/3, -Vdc/3, 0, +Vdc/3, +2Vdc/3, +Vdc\}$

From the above fig.3 :This configuration is highly suitable for medium-voltage drives and photovoltaic systems due to its ability to generate a high-quality stepped waveform[6].

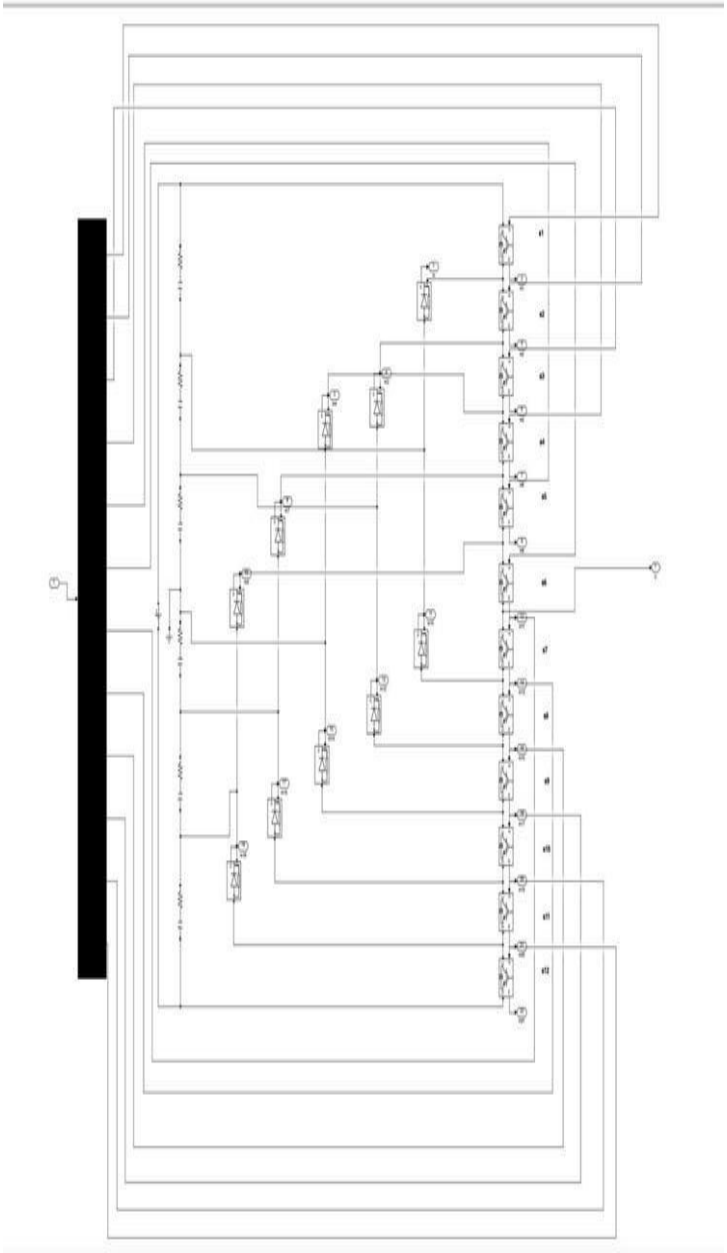

Figure 3: Circuit Configuration of the 7-Level Diode- Clamped Inverter [5]

A. PWM Switching Logic

- Input Signal: The input block (sine or carrier signal) implements the Modified SVPWM with Phase Disposition (PD) logic.

- Lookup Table / Switching Function: A block with 14 inputs (0–13) translates PWM commands into gate signals for 12 switches.
- Switching Vectors: Inputs correspond to switching states for the 7-level output. Redundancy in zero vectors allows neutral-point balancing, critical for DCMLI .[5]

B. Comparison with Cascaded H-Bridge Inverter

Figure 4: Switching Sequence Diagram

DLCMI	Cascaded H Bridge Inverter
Number of switches	2
Switching frequency	High
Size	Larger
Control complexity	Higher

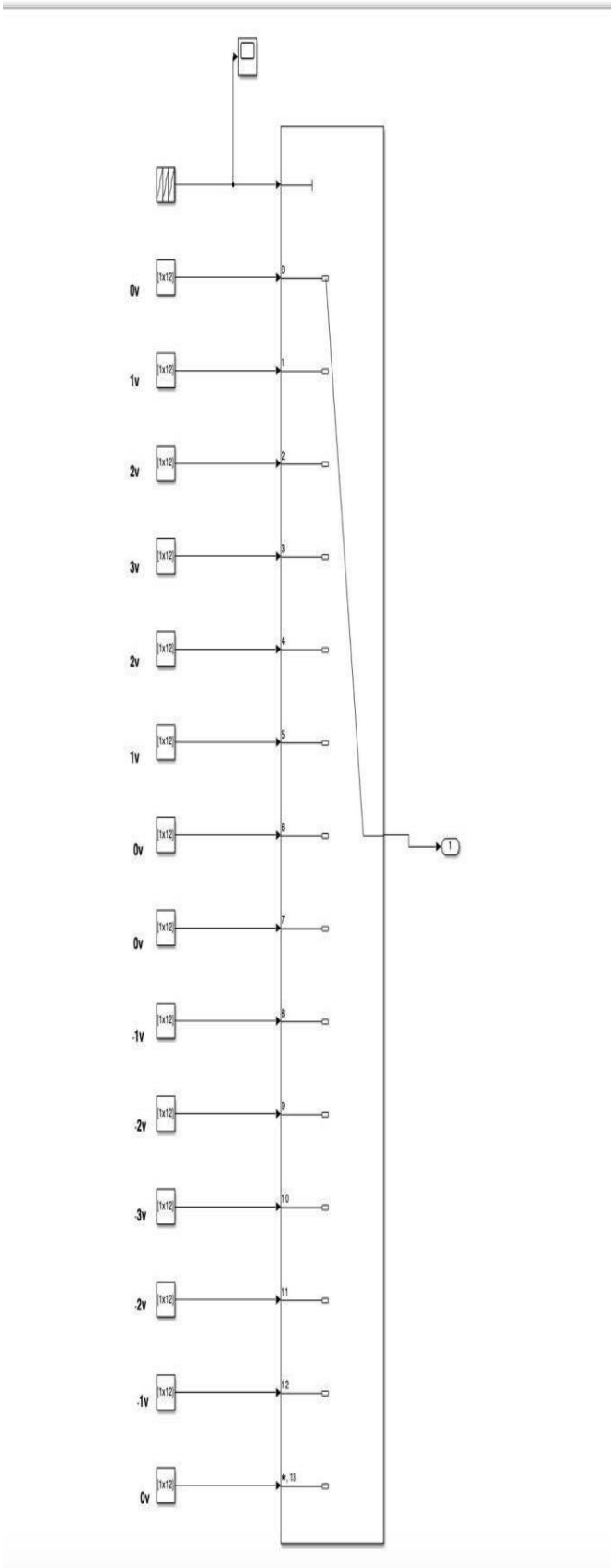
0v
1v
2v
3v
2v
1v
0v
0v
-1v
-2v
-3v
-2v
-1v
0v
1x12
1

Table 1. Switching states of the 7-level DCMLI

sw	S	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12
0v	0	0	0	1	1	1	1	1	1	0	0	0
V1	0	0	1	1	1	1	1	1	0	0	0	0
V2	0	1	1	1	1	1	1	1	0	0	0	0
V3	1	1	1	1	1	1	1	1	0	0	0	0
-v1	0	0	0	0	1	1	1	1	1	1	0	0
-v2	0	0	0	0	0	0	1	1	1	1	1	0
-v3	0	0	0	0	0	0	0	0	1	1	1	1

C. Calculate Time Instants:

Starting from time t=0, add the segment duration repeatedly to find the time instants for the boundaries of each segment.[7]

For example, for a waveform divided into four parts:

- Time instant 1: t = 0
- Time instant 2: t = T/4
- Time instant 3: t = 2T/4 = T/2
- Time instant 4: t = 3T/4
- Time instant 5: t = 4T/4 = T

4. Results and Discussion

Simulation studies in MATLAB/Simulink indicate that Modified SVPWM with PD and trapezoidal carriers achieves the lowest THD of 7.98% for phase voltage. DC link utilization improves by 15–16% compared to conventional SPWM. Experimental validation on a 400 V prototype confirms THD reduction to 0.28% demonstrating significant harmonic mitigation. The phase voltage of the seven-level inverter is synthesized resulting in a staircase waveform that closely approximates a sinusoidal voltage. Compared to conventional two-level and three-level inverters, the seven-level structure provides smoother voltage transitions, thereby minimizing sudden voltage changes (dv/dt)[3][2].

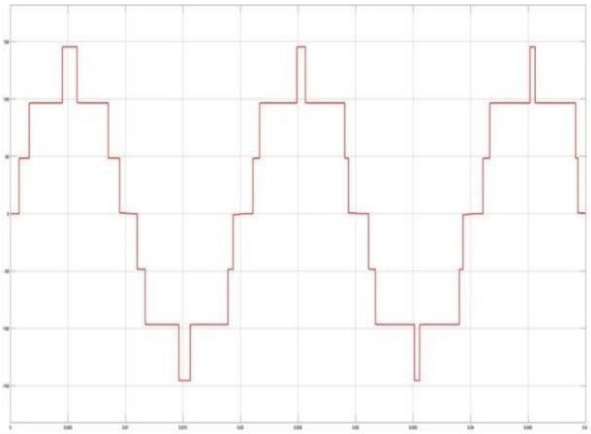

Figure 5: Phase Voltage THD Graph

The Total Harmonic Distortion (THD) of the output voltage is considerably reduced in the seven-level inverter. The presence of multiple voltage levels helps in distributing the harmonic energy over higher-order harmonics, which are easier to filter. As a result, the output voltage THD is significantly lower than that of lower-level inverter .Overall, the simulation results confirm that the diode-clamped seven-level inverter effectively improves power quality by reducing harmonic distortion, enhancing voltage waveform smoothness, and lowering device stress, making it a reliable solution for modern power electronic applications.[1]

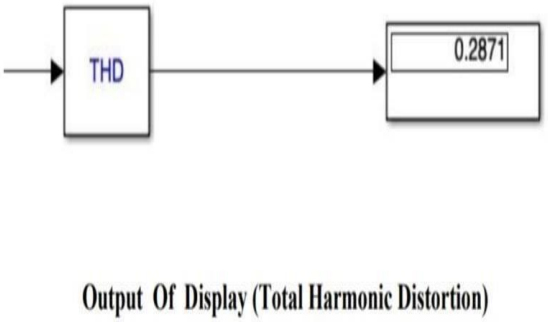

Figure 6 : THD Output

5. Acknowledgment

The authors would like to express their sincere gratitude to the Department of Electrical and Electronics Engineering, RNS Institute of Technology, Bangalore, for providing the necessary facilities and support to carry out this work. The authors are especially thankful to Dr. Rashmi Deepak, Assistant Professor, for her valuable guidance, continuous encouragement, and technical insights throughout the course of this study. The support and cooperation extended by the faculty members of the department are also gratefully acknowledged.

References

1. C. R. Balamurugan, S. P. Natarajan, And R. Revathy, "Performance Evaluation Of Multilevel Inverter," International Journal Of Innovation And Applied Studies, Vol. 3, No. 1, May 2013.
2. K. K. Gupta And S. Jain, "Topology For Multilevel Inverters To Attain A Maximum Number Of Levels From Given
3. Dc Sources," Iet Power Electronics, Vol. 5, No. 4, Pp. 435–446, April 2012.
4. M. Manjrekar And T. Lipo, "A Hybrid Multilevel Inverter Topology For Drive Applications," In Proc. Ieee Applied Power Electronics Conference (Apec), Vol. 2, Pp. 523–529, 1998.
5. P. Steimer And M. Manjrekar, "Practical Medium-Voltage Converter Topologies For High-Power Applications," In Proc. Ieee Industry Applications Society Annual Meeting (Ias), Vol. 3, Pp. 1723–1730, 2001.
6. J. Holtz, "Pulse Width Modulation—A Survey," Ieee Transactions On Industrial Electronics, Vol. 39, No. 5, Pp. 410–420, October 1992.
7. G. Carrara, S. Gardella, M. Marchesoni, R. Salutari, And G. Sciutto, "A New Multilevel Pwm Method: A Theoretical Analysis," Ieee Transactions On Power Electronics, Vol. 7, No. 3, Pp. 497–505, July 1992.
8. P. Palanivel And S. S. Dash, "Analysis Of Thd And Output Voltage Performance For Cascaded Multilevel Inverter Using Carrier Pulse Width Modulation Techniques," Iet Power Electronics, Vol. 4, No. 8, Pp. 951–958, September 2011.
9. W. Yao, H. Hu, And Z. Lu, "Comparisons Of Space-Vector Modulation And Carrier-Based Modulation Of Multilevel Inverter," Ieee Transactions On Power Electronics, Vol. 23, No. 1, Pp. 45–51, January 2008.
10. F. Z. Peng, J. S. Lai, J. W. Mckeever, And J. Van Coevering, "A Multilevel Voltage-Source Inverter With Separate Dc Sources For Static Var Generation," Ieee Transactions On
11. Industry Applications, Vol. 32, No. 5, Pp. 1130–1138, September 1996.