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A Mathematical Framework for Structural Connectivity and Complexity Analysis of Processor Interconnection Networks

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Abstract

Processor interconnection networks provide the communication infrastructure for parallel computing, multiprocessor systems, many-core architectures, distributed computing, and high-performance computing. Their topology directly influences processor connectivity, communication distance, structural redundancy, fault tolerance, scalability, and implementation requirements. A systematic structural analysis is therefore essential for understanding interconnection-network characteristics before topology optimization or intelligent routing is applied.

This paper presents a mathematical framework for the structural connectivity and complexity analysis of processor interconnection networks using graph-theoretic models. An interconnection network is represented as an undirected graph $G = (V, E)$, where vertices represent processors and edges represent communication links. The framework integrates multiple structural measures, including node degree, degree variance, link density, network diameter, average shortest-path length, clustering coefficient, betweenness and closeness centrality, path diversity, connectivity ratio, structural redundancy, and fault-tolerance retention. A normalized Structural Complexity Index (SCI) is formulated to jointly characterize communication distance and link requirements within a common comparative framework.

The framework is demonstrated using five representative processor interconnection topologies: Hypercube, Torus, Fat-Tree, Dragonfly, and Perfect Difference Network (PDN). A 64-node configuration is used as the representative structural demonstration to examine differences in connectivity, communication distance, redundancy, and structural requirements across the selected topologies. The framework provides a unified structural baseline that can be extended to larger processor configurations and failure-oriented studies. Detailed stochastic failure experiments and probabilistic reliability estimation are beyond the scope of the present study.

Processor interconnection networks, graph theory, network topology, structural connectivity, structural complexity, path diversity, fault tolerance, graph-based analysis, Structural Complexity Index.

1. Introduction

The increasing demand for parallel and distributed computing has resulted in processor systems containing a large number of interconnected processing elements. In such systems, processors must exchange data through an underlying communication network. The interconnection network therefore becomes an important determinant of overall system performance, scalability, reliability, and communication efficiency (**b20?**; **b21?**; **b26?**).

An interconnection network can be viewed as a structured collection of processors and communication links. Different network topologies provide different combinations of node degree, communication distance, redundancy, fault tolerance, implementation complexity, and scalability (**b20?**; **b21?**; **b26?**). A topology with a large number of communication links can provide multiple alternative communication paths and improved resilience, but it may also require greater hardware resources and routing complexity. Conversely, a sparse topology may reduce implementation requirements while increasing communication distance and vulnerability to failures (**b13?**; **b14?**; **b26?**).

Interconnection-network topology is therefore not merely a structural choice. It influences communication behavior, resilience, scalability, and the ability of the system to continue operation under component failures. Reliability-constrained network design studies similarly model processors as nodes and communication links as edges and consider connectivity, redundancy, reliability, and cost as important design factors (**b1?**; **b2?**; **b4?**; **b5?**).

Before optimizing an interconnection network or applying artificial intelligence techniques to routing, it is necessary to understand the structural characteristics of the underlying topology. A systematic structural study can answer questions such as:

1. How does processor connectivity change as network size increases?
2. Which topologies provide shorter communication paths?
3. How does structural redundancy influence fault tolerance?
4. Which topologies provide a favorable balance between connectivity and structural complexity?
5. How does network structure affect reliability under processor or link failures?
6. Which structural characteristics can subsequently be used as inputs to optimization and AI-based routing methods?

This paper addresses these questions through a graph-theoretic comparative study of representative processor interconnection topologies.

1.1 Motivation

The motivation for this study arises from the observation that connectivity, complexity, and reliability are strongly coupled.

Increasing the number of links can improve redundancy and alternative routing paths, but it can also increase structural complexity. Similarly, reducing the diameter of a network can improve communication efficiency while requiring a topology with higher connectivity or more complex organization.

Therefore, evaluating a topology using a single metric is insufficient. A topology may have a low diameter but relatively high degree, or strong regularity but greater average communication distance. A multi-metric structural analysis is consequently required.

1.2 Research Problem

The central research problem considered in this paper is:

How can the structural characteristics of different processor interconnection network topologies be systematically characterized in terms of connectivity, communication distance, redundancy, complexity, scalability, and reliability-related measures?

1.3 Research Objectives

The objectives of this study are:

1. To represent processor interconnection networks using graph-theoretic models.
2. To formulate quantitative measures for network connectivity and structural complexity.
3. To analyze communication distance using diameter and average shortest-path length.
4. To investigate structural redundancy and path diversity.
5. To formulate structural measures for assessing robustness and reliability under potential processor and link failures.
6. To compare representative processor interconnection topologies under different network sizes.
7. To identify structural characteristics that can support subsequent topology optimization and AI-based routing.

1.4 Contributions

The main contributions of this paper are:

- A unified graph-theoretic representation of processor interconnection networks.
- A systematic structural characterization based on connectivity, distance, density, redundancy, and centrality measures.
- A comparative framework for assessing Hypercube, Torus, Fat-Tree, Dragonfly, and Perfect Difference Network topologies.
- A structural complexity assessment incorporating communication distance and link requirements.
- A structural formulation of robustness and fault-tolerance measures that can support subsequent failure-based analysis.
- A structural baseline that can support subsequent topology optimization and AI-based adaptive routing.

2. Background and Related Work

2.1 Processor Interconnection Networks

An interconnection network defines the communication structure among processors. The topology determines which processors can communicate directly and how messages travel between non-adjacent processors.

Representative topologies include regular structures such as Hypercube and Torus and hierarchical or high-radix structures such as Fat-Tree and Dragonfly (**b20?**; **b21?**; **b26?**). Perfect Difference Network (PDN) provides another structured topology for processor interconnection (**b6?**).

Each topology exhibits different structural characteristics. Hypercube networks provide regular connectivity and logarithmic diameter. Torus networks provide regular organization but may exhibit greater communication distances as the network grows. Fat-Tree provides hierarchical connectivity, while Dragonfly is designed to provide short communication distances and high path diversity (**b19?**; **b20?**; **b21?**; **b26?**).

2.2 Graph-Theoretic Representation

An interconnection network can be represented as an undirected graph $G = (V, E)$ (**b27?**), where V represents the set of processors and E represents the set of communication links.

This representation enables standard graph algorithms to be applied to processor networks, including shortest-path analysis, connectivity analysis, centrality analysis, and failure analysis.

2.3 Research Gap

Existing studies have investigated topology optimization under reliability constraints (**b4?**; **b5?**), structural and diagnosability properties of interconnection networks (**b7?**; **b8?**), genetic-algorithm-based topology optimization (**b9?**; **b11?**), and graph-reliability characterization and bounds (**b13?**; **b14?**; **b15?**). However, these studies generally address individual aspects of interconnection-network structure rather than providing a unified framework integrating connectivity, communication distance, redundancy, scalability, and reliability-related structural measures.

There is therefore a need for a unified structural study that places connectivity, communication complexity, redundancy, scalability, and reliability within a common analytical framework.

This paper addresses this requirement by establishing a structural baseline across multiple processor interconnection topology families.

3. Mathematical Model of Processor Interconnection Networks

3.1 Network Graph

Let the processor interconnection network be represented by

$$G = (V, E)$$

where

$$V = \{v_1, v_2, \dots, v_N\}$$

and

$$E = \{(v_i, v_j) \mid v_i, v_j \in V\}.$$

Here, $N = |V|$ represents the number of processors and $M = |E|$ represents the number of communication links.

3.2 Node Degree

The degree of processor v_i is

$$d(v_i) = |\{v_j : (v_i, v_j) \in E\}|.$$

The average node degree is

$$\bar{d} = \frac{1}{N}\sum_{i=1}^{N} d(v_i).$$

For an undirected graph,

$$\boxed{\bar{d} = \frac{2M}{N}}$$

The average degree provides an indication of the connectivity requirement of a topology.

3.3 Degree Variance

Degree variance measures the uniformity of processor connectivity:

$$\sigma_d^2 = \frac{1}{N}\sum_{i=1}^{N} (d(v_i) - \bar{d})^2.$$

A low value indicates a relatively regular topology, whereas a high value indicates heterogeneous connectivity.

3.4 Link Density

The link density of an undirected graph is

$$LD = \frac{2M}{N(N-1)}.$$

A higher density indicates that a larger fraction of the possible processor-to-processor links is present.

3.5 Network Diameter

The network diameter is defined as

$$D(G) = \max_{u,v \in V} d(u, v),$$

where $d(u, v)$ is the shortest-path distance between processors u and v.

A smaller diameter generally indicates a smaller worst-case communication distance.

3.6 Average Shortest-Path Length

The average shortest-path length is

$$L(G) = \frac{1}{N(N-1)} \sum_{u \neq v} d(u, v).$$

This metric represents the average communication distance between processor pairs.

3.7 Connectivity

A network is connected if a path exists between every pair of processors.

The binary connectivity indicator is

$$C(G) = \begin{cases} 1, & G \text{ is connected,} \\ 0, & G \text{ is disconnected.} \end{cases}$$

For failure experiments, the connectivity ratio is defined as

$$CR = \frac{|V_c|}{|V|}$$

where V_c represents the processors belonging to the largest connected component.

3.8 Path Diversity

For a processor pair (u, v), let k_{uv} represent the number of edge-disjoint paths between the processors.

A network-level path-diversity measure can be expressed as

$$PD = \frac{1}{P} \sum_{(u,v)} k_{uv},$$

where P is the number of evaluated processor pairs.

Path diversity represents the availability of alternative communication routes.

4. Connectivity, Complexity, and Reliability Metrics

4.1 Connectivity Dimension

Connectivity is evaluated using:

- Average degree
- Minimum degree
- Connectivity ratio
- Number of connected components
- Edge connectivity
- Vertex connectivity
- Path diversity

These measures provide complementary information about network robustness.

4.2 Communication Complexity

Communication complexity is represented through:

- Network diameter
- Average shortest-path length
- Node degree
- Link density
- Betweenness centrality

A network with a small diameter and low average path length can potentially reduce communication distance, while a high degree may increase routing alternatives but also increase structural requirements.

4.3 Structural Redundancy

For a connected graph, a spanning tree contains $N - 1$ edges. Therefore, the number of surplus edges can be defined as

$$R_E(N) = M(N) - (N - 1).$$

For a fixed processor count N, a normalized structural redundancy measure is defined as

$$SR(N) = \frac{M(N) - (N - 1)}{M_{max}(N) - (N - 1)}.$$

This quantity is used as a structural redundancy indicator and should not be interpreted as exact probabilistic reliability.

4.4 Betweenness Centrality

The betweenness centrality of processor v is

$$BC(v) = \sum_{s \neq v \neq t} \frac{\sigma_{st}(v)}{\sigma_{st}},$$

where σ_{st} is the number of shortest paths between s and t, while $\sigma_{st}(v)$ is the number of those paths passing through v.

A high value indicates that a processor has a significant role in shortest-path communication.

4.5 Closeness Centrality

The closeness centrality of processor v is defined as

$$CL(v) = \frac{N - 1}{\sum_{u \in V,\, u \neq v} d\,(v, u)}.$$

A higher closeness centrality indicates that a processor is, on average, at a shorter graph distance from the other processors. This measure provides an additional representation of the processor's accessibility within the network.

4.6 Clustering Coefficient

The local clustering coefficient of node v is

$$\mathrm{CC(v)} = \frac{2\mathrm{T(v)}}{\mathrm{d(v)(d(v)-1)}}$$

where $\mathrm{T(v)}$ is the number of triangles involving v. For nodes with $\mathrm{d(v)} < 2$, the local clustering coefficient is defined as zero.

The network clustering coefficient is obtained by averaging the local values.

4.7 Fault Tolerance

Fault tolerance is defined as the ability of a processor interconnection network to retain structural connectivity after processor or communication-link failures. For a specified failure level f, the connectivity-retention measure is defined as

$$\mathrm{FT(f)} = \frac{\mathrm{CR_f}}{\mathrm{CR_0}},$$

where $\mathrm{CR_0}$ is the initial connectivity ratio and $\mathrm{CR_f}$ is the connectivity ratio after the specified failure condition. For a fully connected initial network, $\mathrm{CR_0} = 1$, and therefore $0 \leq \mathrm{FT(f)} \leq 1$.

In this paper, the metric is formulated as part of the structural analysis framework. Detailed failure-based evaluation is outside the primary scope of the present structural study and can be performed in subsequent reliability and adaptive-routing studies.

5. Structural Complexity Model

Structural complexity should not be interpreted solely in terms of the number of communication links. It also reflects the communication distance and the structural requirements imposed by a topology.

For comparative analysis at a given processor count N, the maximum reference values are defined over the set of evaluated topologies $\mathcal{T}$ as

$$\mathrm{D_{max}(N)} = \max_{\mathrm{T}\in\mathcal{T}} \mathrm{D_T(N)},$$

$$\mathrm{L_{max}(N)} = \max_{\mathrm{T}\in\mathcal{T}} \mathrm{L_T(N)},$$

and

$$\mathrm{M_{max}(N)} = \max_{\mathrm{T}\in\mathcal{T}} \mathrm{M_T(N)},$$

where $\mathcal{T}$ denotes the set of evaluated topologies, namely Hypercube, Torus, Fat-Tree, Dragonfly, and Perfect Difference Network (PDN).

The corresponding normalized structural measures are

$$D_n(N) = \frac{D(N)}{D_{max}(N)},$$

$$L_n(N) = \frac{L(N)}{L_{max}(N)},$$

and

$$M_n(N) = \frac{M(N)}{M_{max}(N)}.$$

The Structural Complexity Index (SCI) is proposed as a comparative graph-structural indicator for relating communication distance and link requirements. It is not intended to represent physical hardware complexity directly. Its purpose within the present study is to provide a common normalized framework that can subsequently be evaluated and refined using topology optimization and application-oriented performance studies.

$$SCI = w_1 D_n + w_2 L_n + w_3 M_n,$$

subject to

$$w_1 + w_2 + w_3 = 1, \qquad w_i \geq 0.$$

Here, w_1, w_2, and w_3 represent the relative importance assigned to communication diameter, average communication distance, and link requirements, respectively.

Unless otherwise specified, equal weighting may be used as the baseline condition:

$$w_1 = w_2 = w_3 = \frac{1}{3}.$$

The corresponding structural efficiency is defined as

$$SE = \frac{1}{1 + SCI}.$$

A larger value of SCI represents higher normalized structural complexity, whereas a larger value of SE represents greater structural efficiency.

6. Proposed Structural Analysis Framework

The proposed framework consists of six stages.

6.1 Stage 1: Topology Generation

Generate the selected processor interconnection topology for a specified number of processors.

6.2 Stage 2: Graph Construction

Represent the topology as

$$G = (V, E).$$

6.3 Stage 3: Structural Measurement

Calculate:

- Number of nodes
- Number of edges
- Average degree
- Degree variance
- Link density
- Diameter
- Average shortest-path length
- Clustering coefficient
- Betweenness centrality
- Path diversity

6.4 Stage 4: Connectivity and Reliability Characterization

Evaluate baseline connectivity and formulate structural robustness measures including connectivity ratio, path diversity, surplus edges, edge connectivity, vertex connectivity, and fault-tolerance retention. Failure-based evaluation can subsequently be applied using these measures.

6.5 Stage 5: Complexity Assessment

Calculate normalized structural metrics and the proposed SCI.

6.6 Stage 6: Comparative Analysis

Compare the evaluated topologies according to:

- Connectivity
- Communication distance
- Redundancy
- Reliability-related structural measures
- Fault tolerance
- Scalability
- Structural complexity

7. Structural Analysis Methodology

7.1 Evaluated Topologies

The study considers five representative processor interconnection topologies:

1. Hypercube
2. Torus

3. Fat-Tree
4. Dragonfly
5. Perfect Difference Network (PDN)

7.2 Representative Network Sizes

The proposed structural framework is applicable to different processor counts. A 64-node configuration is used as the representative structural demonstration in the present study. The framework can be extended to larger configurations, including 128, 256, and 512 nodes, which are reserved for subsequent experimental studies.

$$N \in \{64,128,256,512\}$$

7.3 Computational Implementation

The proposed graph-theoretic framework can be implemented using standard scientific-computing and graph-analysis libraries. A reference implementation may use Python 3.11 together with NetworkX, NumPy, SciPy, Pandas, and Matplotlib for topology generation, graph construction, metric calculation, and visualization.

7.4 Structural Metric Evaluation

The proposed framework defines the following graph-based characteristics for evaluating each selected topology and representative processor configuration:

- number of processors and communication links,
- average and minimum node degree,
- degree variance,
- link density,
- network diameter,
- average shortest-path length,
- clustering coefficient,
- betweenness and closeness centrality,
- path diversity,
- structural redundancy, and
- the proposed Structural Complexity Index.

These measures provide a unified structural description of the selected processor interconnection topologies.

7.5 Reliability and Failure Analysis Scope

Reliability and fault tolerance are incorporated into the framework through structural robustness measures. These measures provide a mathematical basis for subsequent failure-oriented analysis; however, detailed stochastic failure experiments and probabilistic reliability estimation are outside the scope of the present structural study.

8. Results and Comparative Analysis

8.1 Basic Structural Properties

Table 1 summarizes representative structural characteristics of the selected topologies for a 64-node configuration. The values provide a representative structural demonstration of the proposed graph-theoretic metrics and illustrate the differences among the selected topology classes. They are not intended to constitute an exhaustive performance evaluation.

Structural Characteristics of Evaluated Topologies for 64 Nodes

Topology	N	M	$\bar{d}$	D	L	PD
Hypercube	64	192	6.0000	6	3.0476	0.5714
Torus	64	128	4.0000	8	4.0635	0.2540
Fat-Tree	64	63	1.9688	6	4.5055	0.0615
Dragonfly	64	240	7.5000	4	2.9365	0.8929
PDN	64	192	6.0000	6	3.4603	0.5714

The evaluated 64-node configurations demonstrate substantial differences among the topology classes. Dragonfly exhibits the smallest diameter and average shortest-path length among the configurations, while Torus has a larger diameter and Fat-Tree has the largest average path length in the evaluated configuration.

Hypercube and PDN exhibit comparable average degree and path-diversity values in the considered configuration. These observations indicate that topology quality cannot be represented using a single structural metric.

8.2 Structural Robustness Characterization

The present study defines structural robustness measures to establish a common analytical basis for subsequent reliability and fault-tolerance investigations. Path diversity and surplus edges characterize structural redundancy, whereas connectivity ratio and fault-tolerance retention provide measures that can be applied when processor or communication-link failures are introduced. These measures are therefore included as part of the proposed structural analysis framework rather than as empirical failure results in the present study.

Structural Robustness Metrics Defined for the Study

Metric	Purpose
Path Diversity (PD)	Measures the average number of edge-disjoint paths available between processor pairs.
Connectivity Ratio (CR)	Measures the fraction of processors retained in the largest connected component under a specified network condition.
Fault-Tolerance Retention (FT)	Measures connectivity retention after failures as $FT(f) = CR_f/CR_0$.
Surplus Edges (R_E)	Measures structural redundancy beyond the minimum $N - 1$ edges required for a connected graph.
Edge Connectivity ($\lambda(G)$)	Represents the minimum number of edges whose removal disconnects the network.

Metric	Purpose
Vertex Connectivity ($\kappa(G)$)	Represents the minimum number of processor vertices whose removal disconnects the network.

8.3 Scalability Analysis

For a structural metric M, the relative change between two network sizes is defined as

$$SC_M = \frac{M(N_2) - M(N_1)}{M(N_1)}.$$

This measure enables comparison of how rapidly structural characteristics change as the number of processors increases.

The scalability analysis investigates:

- Diameter growth
- Average path-length growth
- Degree variation
- Path-diversity variation
- Structural-complexity growth

9. Discussion

The structural analysis demonstrates that processor interconnection topologies exhibit fundamentally different relationships among connectivity, communication distance, redundancy, and reliability.

A topology with a higher node degree generally provides more direct communication opportunities and potentially more alternative routes. However, higher connectivity also implies additional links and greater structural requirements. This establishes a fundamental trade-off between redundancy and structural complexity.

Diameter and average shortest-path length provide different information. Diameter describes the worst-case communication distance, whereas average shortest-path length represents the overall communication-distance behavior. Consequently, both metrics should be considered when evaluating topology efficiency.

Path diversity provides another important dimension. A topology may have a small diameter but insufficient alternative routes for some processor pairs. Conversely, a topology with higher path diversity may provide improved resilience under link failures.

The results therefore support a multi-dimensional view of processor interconnection-network analysis rather than ranking topologies using a single metric.

10. Relationship with Topology Optimization and AI-Based Routing

The primary purpose of this paper within the overall research program is to establish a structural foundation.

The graph representation developed here directly supports the topology optimization formulation used in the subsequent Improved Genetic Algorithm study.

In that formulation, processors are represented as graph nodes and candidate communication links as graph edges, while link-level cost and reliability are associated with the candidate links.

The structural metrics developed in this study also provide useful features for AI-based routing. The subsequent AICOF framework uses graph-derived characteristics including degree, betweenness centrality, clustering coefficient, and closeness centrality together with dynamic traffic and failure information.

Thus, the three studies form a coherent research sequence, as illustrated in Fig. 1.

→ →

Research progression from structural study to topology optimization and AI-based adaptive routing.

Paper-1 establishes what the network looks like.

Paper-2 investigates how its topology can be optimized.

Paper-3 investigates how routing can intelligently adapt to network conditions.

11. Implications for AI-Based Network Optimization

The structural study has an important implication for artificial intelligence.

AI models require meaningful representations of the system state. In networked systems, graph-based representations provide a natural mechanism for capturing relationships among nodes and links (**b22?**; **b23?**; **b24?**).

In the subsequent AICOF framework, structural graph features are combined with dynamic network information for MLP, GNN, and reinforcement-learning components (**b22?**; **b24?**).

A structural feature vector can therefore be represented as

$$X_s = [d(v), BC(v), CC(v), CL(v), D, L, PD, CR].$$

These structural characteristics can subsequently be combined with dynamic variables such as:

- Processor load
- Link utilization
- Queue length
- Congestion
- Failure state

The resulting representation provides a bridge between classical graph analysis and intelligent network management.

12. Limitations

The following limitations are acknowledged:

1. The analysis is primarily graph-structural and does not model complete physical implementation overhead.
2. Structural reliability measures should not be interpreted as exact probabilistic all-terminal reliability unless an appropriate probabilistic model is explicitly implemented (**b13?**; **b14?**; **b15?**; **b16?**).
3. The proposed Structural Complexity Index depends on normalization and weighting parameters.
4. The current structural demonstration is limited to the selected topology families and representative network configurations.
5. The framework does not include detailed traffic, congestion, energy, or application-level performance evaluation.
6. Failure-based and probabilistic reliability evaluation requires additional stochastic experiments and is reserved for subsequent studies.

13. Future Work

Future research can extend this study in several directions:

1. Evaluation of larger processor counts.
2. Investigation of additional interconnection topologies.
3. Probabilistic all-terminal and k-terminal reliability analysis.
4. Multi-objective topology optimization using the structural metrics developed in this study.
5. Integration of graph neural networks for topology representation.
6. Reinforcement-learning-based adaptive routing.
7. Hardware-oriented cost and energy modeling.
8. Dynamic failure and congestion scenarios.
9. Real-world HPC and many-core application traces.
10. Development of topology-aware AI models using structural features.

14. Conclusion

This paper presented a graph-theoretic study of processor interconnection networks with emphasis on connectivity, complexity, redundancy, scalability, and reliability. The interconnection network was represented as an undirected graph in which processors correspond to vertices and communication links correspond to edges. A unified set of structural metrics was formulated to characterize processor connectivity, communication distance, link density, redundancy, centrality, path diversity, and fault tolerance.

Five representative processor interconnection topologies—Hypercube, Torus, Fat-Tree, Dragonfly, and Perfect Difference Network—were considered for comparative structural analysis. The study demonstrates that different topologies exhibit different trade-offs among communication distance, connectivity, redundancy, and structural requirements. Consequently, no single structural metric is sufficient for comprehensive evaluation of an interconnection network.

The study provides a foundational structural characterization that can support subsequent topology optimization and intelligent routing research. In the broader research framework, the present study establishes the structural characteristics of processor interconnection networks; the subsequent work applies an Improved Genetic Algorithm to optimize topology under reliability and cost constraints; and the later AICOF framework uses graph-based structural information together with dynamic network conditions for AI-assisted adaptive routing.

Therefore, the overall research progression can be summarized as

Study → Optimize → Intelligently Adapt

This establishes a coherent graph-theoretic and computational foundation for studying connectivity and complexity of processor structures in interconnection networks using artificial intelligence techniques.

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