

A Systematic Framework for Fault Diagnosis and Troubleshooting in Electronics Engineering Laboratories: Methods, Validation, and Practical Applications

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Abstract

Electronics engineering laboratories support the development of practical competence in circuit construction, measurement, interpretation, and fault diagnosis. However, troubleshooting can become inconsistent when students and laboratory personnel rely on trial-and-error component replacement, incomplete documentation, or measurements taken without a defined diagnostic sequence. This paper proposes a systematic, safety-oriented framework for diagnosing and resolving faults in Electronic Devices and Circuits (EDC), digital electronics, and analog electronics laboratories. The framework integrates eight stages: (1) symptom definition, (2) safety and visual inspection, (3) functional decomposition, (4) hypothesis generation, (5) measurement planning, (6) controlled testing, (7) corrective action, and (8) post-repair verification and documentation. Its practical use is illustrated through representative fault scenarios involving power-supply instability, semiconductor biasing, logic trainer kits, and analog signal-conditioning circuits. A set of performance indicators is also defined to support future empirical evaluation, including diagnostic time, first-pass resolution, recurrence rate, and completeness of maintenance records. The paper is a framework-development contribution rather than a report of a completed controlled experiment; therefore, it does not claim measured improvements in student performance or equipment reliability. The proposed framework provides a reproducible basis for laboratory troubleshooting practice and future validation across engineering institutions.

Keywords: electronics laboratory; fault diagnosis; troubleshooting; engineering education; electronic devices and circuits; digital electronics; analog electronics; maintenance documentation

1. Introduction

Engineering laboratory learning depends not only on assembling a circuit correctly but also on recognising abnormal behaviour, identifying likely causes, selecting suitable measurements, and verifying corrective action. In electronics laboratories, faults may originate from component failure, incorrect wiring, poor contacts, unsuitable instrument settings, power-supply problems, thermal stress, or misunderstanding of circuit operation. A troubleshooting method that is systematic and documented can

reduce avoidable component damage and help distinguish a circuit fault from a measurement or setup error.

Prior work in physics and engineering education identifies troubleshooting as an important laboratory learning outcome, while also noting that students may move directly to testing or repair without sufficiently planning their diagnosis [1–3]. Research on electronics-laboratory instruction has similarly highlighted differences between instructors' stated priorities and the extent to which troubleshooting is explicitly taught and assessed [1]. These findings support the need for a transparent process that makes diagnostic reasoning visible and assessable.

This paper focuses on three connected laboratory domains: Electronic Devices and Circuits (EDC), digital electronics, and analog electronics. Although these domains use different circuit models and instruments, they share a common diagnostic logic: establish the expected behaviour, observe the symptom, isolate the faulty stage, test hypotheses with controlled measurements, correct the verified cause, and confirm normal operation.

The contribution is a practical eight-stage framework and a set of domain-specific diagnostic matrices. It is intended for laboratory technicians, instructors, and engineering students. The framework is presented as a structured proposal; empirical effectiveness must be established through a future implementation study using recorded baseline and post-implementation data.

2. Background and Related Work

2.1 Troubleshooting as a reasoning activity

Troubleshooting is not simply the replacement of a suspected component. It is a reasoning process in which the troubleshooter builds and revises a model of how the system should behave, compares that model with observations, and chooses tests that discriminate among possible causes. Dounas-Frazer and Lewandowski reported that electronics laboratory instructors regard troubleshooting as an important learning outcome, while practices for directly assessing it vary [1]. Dounas-Frazer and colleagues also examined the relationship between model-based reasoning and troubleshooting in electric circuits [2].

2.2 Student approaches and diagnostic planning

A recent qualitative investigation of introductory students troubleshooting an electronic circuit found that participants often moved quickly into testing and repair, while earlier activities such as understanding system function, generating possible causes, and planning a diagnostic sequence received less attention [3]. This observation is relevant to laboratory practice because unplanned probing may produce ambiguous results, overlook upstream faults, or introduce additional damage.

2.3 Practical gap addressed by this framework

The proposed framework translates general troubleshooting principles into a workflow suitable for routine EDC, digital, and analog laboratory activities. It explicitly includes safety checks, measurement-point selection, evidence-based fault isolation, post-repair verification, and documentation. Unlike a device-specific service manual, it is designed to be reusable across laboratory exercises and equipment types.

3. Aim, Objectives, and Research Questions

The aim is to develop a repeatable framework for fault diagnosis and troubleshooting in electronics engineering laboratories.

The objectives are: (i) to define a staged diagnostic workflow; (ii) to map common fault symptoms to plausible causes and discriminating tests in EDC, digital electronics, and analog electronics; (iii) to define measurable indicators for evaluating troubleshooting practice; and (iv) to specify a validation approach that can be used in a subsequent laboratory study.

The paper is guided by three questions: RQ1: How can troubleshooting be structured into a repeatable workflow across different electronics laboratory domains? RQ2: Which diagnostic actions and records should be included to support safe, evidence-based fault isolation? RQ3: Which indicators can be used in future studies to evaluate the framework's operational and educational value?

4. Method and Framework Development

4.1 Design approach

This is a conceptual framework-development paper informed by published research on troubleshooting instruction and electronic-circuit diagnosis [1–3], together with established engineering reasoning principles: safety before energisation, measurement against expected behaviour, isolation of variables, and verification after corrective action. No human-participant experiment, controlled comparison, or quantitative intervention was conducted for this manuscript. Consequently, the framework is not presented as empirically validated.

4.2 Eight-stage troubleshooting framework

Stage	Purpose	Required actions	Record/output
1. Define the symptom	Describe the deviation clearly	Record the observed symptom, operating condition, and expected behaviour; avoid premature conclusions	Symptom statement
2. Safety and visual inspection	Prevent injury and secondary damage	Isolate power where appropriate; inspect leads, connectors, polarity, solder joints, overheating, and visible damage	Safety/inspection checklist
3. Decompose the system	Identify functional blocks and signal/power paths	Review circuit diagram, pinout, supply rails, bias points, clock/reset paths, and expected signal flow	Annotated circuit or block diagram

4. Generate hypotheses	Create plausible, testable explanations	List likely causes and rank them by evidence, risk, and ease of testing	Prioritised fault hypotheses
5. Plan measurements	Select tests that distinguish hypotheses	Choose instrument, range, reference point, test point, expected value, and safe operating condition	Measurement plan
6. Test and isolate	Gather evidence under controlled conditions	Change one variable at a time; compare measurements with calculated or specified values; isolate the faulty stage	Measurement log and narrowed cause
7. Correct the verified cause	Restore intended operation	Repair wiring/contact issues or replace a confirmed defective part using approved procedures; avoid speculative replacement	Corrective-action record
8. Verify and document	Confirm stable operation and prevent recurrence	Repeat functional tests; check relevant operating conditions; record final readings, parts, date, and follow-up needs	Verification and maintenance record

The stages are sequential for traceability but may be revisited when evidence contradicts the current hypothesis. A failed verification returns the process to measurement planning or hypothesis generation rather than being recorded as a successful repair.

4.3 Decision rules and measurement discipline

Measurements should be selected to reduce uncertainty rather than to accumulate readings. For each test, the operator should state the question being answered, the expected range or logical state, and the result that would support or weaken each hypothesis. Before probing a live circuit, the operator must confirm instrument category and rating, probe condition, grounding arrangement, and the circuit's voltage/current limits. Power should be removed before changing ICs, rewiring, or making resistance/continuity measurements unless the equipment procedure explicitly requires otherwise.

Where a nominal value is available, deviation may be represented as: Percentage deviation = $\frac{|\text{measured value} - \text{nominal value}|}{|\text{nominal value}|} \times 100\%$. This expression is not appropriate when the nominal value is zero; in such cases, an absolute error or a specified tolerance band should be used. For digital

circuits, logic-level interpretation should follow the relevant IC family's guaranteed input/output specifications rather than treating any measured voltage as a universal HIGH or LOW.

5. Domain-Specific Applications

5.1 Electronic Devices and Circuits (EDC)

EDC experiments commonly involve diodes, rectifiers, transistor biasing, common-emitter amplifiers, and basic power-supply circuits. A useful diagnostic sequence begins with supply and ground checks, followed by component orientation and continuity checks, then DC operating-point measurements, and finally signal measurements. For a transistor amplifier, collector, base, and emitter voltages should be compared with the intended bias region before investigating gain or waveform distortion. Incorrect biasing, a reversed component, an open connection, or a shorted load can all produce similar symptoms; the sequence should therefore isolate causes rather than assume a failed transistor.

5.2 Digital electronics

Digital laboratory faults may appear as a missing output, an incorrect truth-table row, unstable LEDs, or a logic state that changes when a wire or IC is touched. The diagnostic sequence should confirm the trainer supply rails and common ground, IC orientation and pin numbering, input states, enable/clear/preset conditions, clock/reset behaviour, and output loading. For combinational circuits, verify the truth table one input combination at a time. For sequential circuits, inspect the clock and asynchronous control inputs before concluding that the IC is defective. Intermittent indicator behaviour should also prompt checks of loose contacts, switch bounce, and supply instability.

5.3 Analog electronics

Analog circuits are sensitive to operating point, component tolerance, loading, frequency response, and measurement setup. Begin with DC conditions and supply rails before investigating AC amplitude, phase, clipping, noise, or oscillation. Confirm the function generator amplitude, frequency, offset, and output impedance; confirm oscilloscope coupling, probe attenuation, time base, and grounding. A waveform that appears distorted may result from amplifier saturation, an incorrect bias point, excessive load, a misconfigured instrument, or a faulty component. Comparing the signal at successive circuit stages helps isolate the first point at which the expected behaviour is lost.

6. Practical Diagnostic Matrices

Tables 2–4 provide illustrative diagnostic matrices. They are not records of completed repairs or measured outcomes. Actual expected values must be taken from the circuit design, component datasheets, laboratory manual, and equipment specifications.

Table 2. EDC fault diagnosis matrix

Observed symptom	Possible causes	Discriminating tests	Corrective action after confirmation
No output from	No input supply; open	Check source and	Restore

rectifier/supply circuit	fuse/lead; diode orientation or failure; open load	transformer output where applicable; inspect continuity with power isolated; measure DC output safely	supply/connection; replace only the confirmed faulty component; retest under rated load
Transistor amplifier has very low gain	Incorrect bias; wrong pin connection; open coupling/bypass capacitor; excessive loading	Measure DC bias at transistor terminals; compare input/output at a known frequency; inspect component values and wiring	Correct bias/wiring or replace confirmed faulty part; repeat gain and clipping checks
Unexpected clipping or asymmetric waveform	Bias point displaced; supply rail issue; excessive input amplitude; load mismatch	Measure supply rails and DC operating point; reduce input amplitude; compare unloaded/loaded output	Correct the cause and document final waveform conditions
Component becomes unusually hot	Incorrect polarity/pinout; short circuit; overcurrent; excessive dissipation	Switch off promptly; inspect for shorts; verify current-limiting and component ratings before re-energising	Do not continue operating until the cause and safe operating condition are established

Table 3. Digital electronics fault diagnosis matrix

Observed symptom	Possible causes	Discriminating tests	Corrective action after confirmation
All outputs remain LOW/HIGH	Missing supply/ground; wrong IC orientation; enable input inactive; wiring fault	Check supply and ground; verify pinout; test enable and input states against truth table	Correct supply, orientation, or control wiring; retest all input combinations
Incorrect truth-table output	Wrong gate connection; damaged IC; floating input; incorrect interpretation of active-low pin	Apply known input combinations; measure each stage; confirm logic family and active-low controls	Correct wiring or replace confirmed defective IC; repeat complete truth-table test
LEDs flicker or logic state is unstable	Loose jumper; switch bounce; unstable supply; floating input	Inspect connectors; measure supply under operation; use defined pull-up/pull-down states; inspect switch signal	Repair contact or supply issue and stabilise inputs; verify repeatability
Counter/register does not advance	Missing clock; reset/preset asserted;	Observe clock with oscilloscope/logic	Correct clock/control wiring and validate

	incorrect edge or enable condition	probe; verify reset and enable states; check timing and pinout	sequence over multiple cycles
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Table 4. Analog electronics fault diagnosis matrix

Observed symptom	Possible causes	Discriminating tests	Corrective action after confirmation
No visible waveform at output	No supply; generator misconfigured; open connection; incorrect scope setup	Check rails and generator output independently; inspect coupling, probe factor, and ground	Restore correct setup or repair verified circuit fault; confirm with known test signal
Unexpected gain or attenuation	Wrong component value; loading; incorrect feedback path; probe setting error	Measure input/output under defined load; verify resistor/capacitor values and feedback continuity	Correct confirmed component or connection issue and repeat gain measurement
Noise or oscillation	Poor grounding/layout; decoupling problem; feedback instability; instrument pickup	Compare with input shorted as appropriate; inspect grounding and decoupling; probe stages carefully	Improve the verified grounding/decoupling or circuit condition; confirm stable operation
Frequency response differs from expectation	Incorrect component value; source/load impedance; wrong frequency range; parasitic effects	Sweep a defined frequency range; record amplitude and phase; verify source and load conditions	Correct the cause and repeat the sweep using documented settings

7. Evaluation Metrics for Future Validation

To evaluate the framework empirically, a laboratory should record baseline performance before implementation and repeat the same defined tasks after staff or students have been trained in the workflow. Task difficulty, equipment condition, available instruments, time limits, and assessment rubrics should be kept comparable. Where feasible, multiple assessors should use a common rubric and disagreements should be documented.

Metric	Operational definition	Interpretation / caution
Diagnostic time	Elapsed time from fault presentation to evidence-supported identification of the root cause	Report median and spread; define start/end points consistently
First-pass resolution rate	Number of cases correctly resolved without repeated	A resolution must pass the verification test, not merely

	corrective cycles divided by total cases $\times 100$	restore a visible output
Repeat-fault rate	Number of cases in which the same fault recurs within a defined follow-up period divided by resolved cases $\times 100$	State follow-up duration and what counts as the same fault
Diagnostic accuracy	Number of correctly identified root causes divided by total evaluated cases $\times 100$	Use independently established fault labels where possible
Documentation completeness	Completed required record fields divided by all required fields $\times 100$	Define mandatory fields before assessment
Component consumption	Number and type of components replaced per completed diagnostic case	Lower replacement counts are not automatically better if reliability is compromised
Safety-procedure adherence	Number of applicable safety steps completed divided by applicable steps $\times 100$	Serious safety violations should be reported separately, not hidden in an average

For a pre/post study, the analysis should report sample size, missing observations, descriptive statistics, uncertainty intervals, and the statistical test selected before inspecting results. If the same participants complete both assessments, a paired analysis may be appropriate; if independent groups are compared, an independent-group method should be selected based on the data distribution and study design. Effect sizes and confidence intervals should accompany significance tests. No numerical values are reported here because no dataset was collected for this manuscript.

8. Implementation Protocol

A practical implementation can begin with a small set of representative faults across the three domains. Each case should have a documented normal operating condition, an intentionally introduced or independently verified fault, an approved safety procedure, and an answer key identifying the root cause. Fault insertion must be performed by authorised personnel with current and power limits controlled. Students should not be exposed to unsafe mains faults or faults that can cause uncontrolled component failure.

Before each session, laboratory personnel should verify instrument functionality, leads, power supplies, protective devices, and the availability of circuit diagrams and datasheets. During the activity, the learner should maintain a measurement log and state the hypothesis tested by each measurement. At completion, the circuit should pass a predefined functional test and the equipment should be returned to a safe state. Fault history, component replacements, and recurring issues should be entered into the maintenance record.

For an institutional evaluation, the protocol should define inclusion criteria for cases, training duration, assessor roles, data-protection procedures, and the primary outcome measure. If student data are

collected for research publication, institutional ethics requirements and consent procedures should be checked before data collection.

9. Discussion

The main value of the framework is its emphasis on diagnostic discipline. The explicit separation of symptom definition, hypothesis generation, measurement planning, and verification can make troubleshooting decisions more transparent than unstructured trial-and-error. It also connects technical repair with educational assessment: a learner can be evaluated not only on whether the circuit works at the end, but on the quality of the diagnostic reasoning, the safety of the procedure, and the traceability of the evidence.

The framework is intended to be domain-general while allowing domain-specific tests. EDC diagnosis prioritises semiconductor operating points and component orientation; digital diagnosis prioritises defined logic levels, control inputs, clock/reset paths, and truth-table behaviour; analog diagnosis prioritises bias, signal path, loading, frequency, and instrument configuration. This balance may make a common laboratory record usable across different experiments without erasing the technical distinctions among them.

The framework also supports laboratory management. A structured record can reveal recurring failures associated with connectors, supply units, trainer kits, or operating practices. However, such trends can only be established from consistently collected maintenance data; the framework alone does not demonstrate that equipment failure or repair time will decrease. A prospective study is required to test these possible benefits.

10. Limitations and Future Work

This paper presents a conceptual framework and illustrative diagnostic matrices, not a completed empirical evaluation. The framework has not yet been tested across a defined sample of students, laboratory technicians, equipment types, or institutions. The diagnostic matrices are representative and must be adapted to the relevant circuit, datasheet, instrument, and safety requirements. The framework may also require modification for high-frequency, RF, power-electronics, embedded, or automated test environments.

Future work should conduct a pilot study with predefined fault cases in EDC, digital electronics, and analog electronics laboratories. A stronger evaluation would use a transparent rubric, independent verification of root causes, repeat trials, and a comparison group or counterbalanced design where feasible. Results should report diagnostic time, accuracy, first-pass resolution, safety adherence, and documentation completeness, including uncertainty and limitations. Multi-institution replication would be necessary before claiming generalisability.

11. Conclusion

This paper has proposed an eight-stage framework for safe, systematic, and documented troubleshooting in electronics engineering laboratories. By combining symptom definition, safety inspection, functional

decomposition, hypothesis generation, measurement planning, controlled testing, corrective action, and post-repair verification, the framework provides a repeatable process for EDC, digital electronics, and analog electronics activities. Domain-specific matrices and evaluation metrics translate the process into practical laboratory use and future research. The framework should be treated as a testable proposal rather than a proven intervention. Its effectiveness must be established through prospective implementation, transparent data collection, and independent verification of outcomes.

Declarations

Funding

The author received no specific external funding for the preparation of this manuscript.

Conflict of Interest

The author declares that there is no known competing financial or non-financial interest that could have influenced the work reported in this manuscript.

Ethics Approval

This manuscript presents a conceptual framework and does not report research involving human participants, identifiable personal data, or live animal subjects. Ethics approval was therefore not applicable to the work reported here. Any future study involving students or staff will follow the relevant institutional ethics requirements before data collection.

Informed Consent

Not applicable to this conceptual paper. Informed consent will be obtained where required for future research involving human participants.

Data Availability

No dataset was generated or analysed for this conceptual framework paper. Data availability provisions will be updated if empirical validation is conducted.

Author Contributions

Dwarakeesh S: Conceptualization, framework development, investigation of relevant literature, writing—original draft, and writing—review and editing.

Acknowledgements

The author acknowledges the broader engineering laboratory education community whose published work informs the discussion of troubleshooting and diagnostic reasoning. No individual or organisation is being represented as having endorsed or validated the proposed framework.

References

1. D. R. Dounas-Frazer and H. J. Lewandowski, “Electronics lab instructors’ approaches to troubleshooting instruction,” *Physical Review Physics Education Research*, vol. 13, no. 1, 010102, 2017. doi: 10.1103/PhysRevPhysEducRes.13.010102.
2. D. R. Dounas-Frazer, K. L. Van De Bogart, M. R. Stetzer, and H. J. Lewandowski, “Investigating the role of model-based reasoning while troubleshooting an electric circuit,”

Physical Review Physics Education Research, vol. 12, 010137, 2016. doi: 10.1103/PhysRevPhysEducRes.12.010137.

3. P. Herbert and T. O'Mahony, "An exploratory qualitative investigation into how introductory students troubleshoot an electronic circuit," *International Journal of Engineering Pedagogy (iJEP)*, vol. 14, no. 8, pp. 139–152, 2024. doi: 10.3991/ijep.v14i8.48319.
4. F. Aveta and Y. Yang-Keathley, "Troubleshooting lab for circuit courses in the electrical and computer engineering program," in *Proceedings of the 2025 ASEE Annual Conference & Exposition*, Montreal, Canada, 2025. doi: 10.18260/1-2--57723.